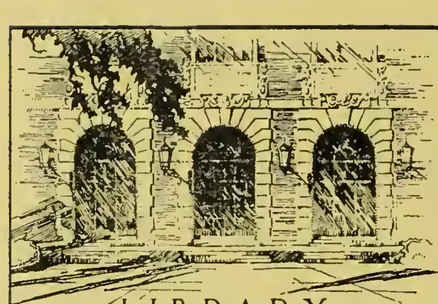

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REPORT NO. 154

DESIGN OF THE PROGRAM-CONTROLLED SEMICONDUCTOR AND PRINTED CIRCUIT BOARD TEST CONSOLE

by

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INTRODUCTION

The design is given here of a test console which measures, under computer control, physical data on components and circuits, and transmits this data back to the controlling computer. This test console, in conjunction with a digital computer, can be used to design circuits or networks directly from empirical data, test previously designed circuits, and classify circuit components under given criteria. A test console of this type should prove helpful to circuit designers and computer fabricators.

This paper consists of two parts: (1) system description, and (2) engineering design.

1. SYSTEM DESCRIPTION

1.1 A Brief View of the Test Console

The Test Console was explicitly designed to be connected to ILLIAC II at the Digital Computer Laboratory; therefore, a word length of 52 bits was selected. All data are transported from ILLIAC II through an interplay channel to the Test Console and vice versa. Control information exchanged between the Test Console and the computer is indicated in Figs. 1(a) and 1(b).

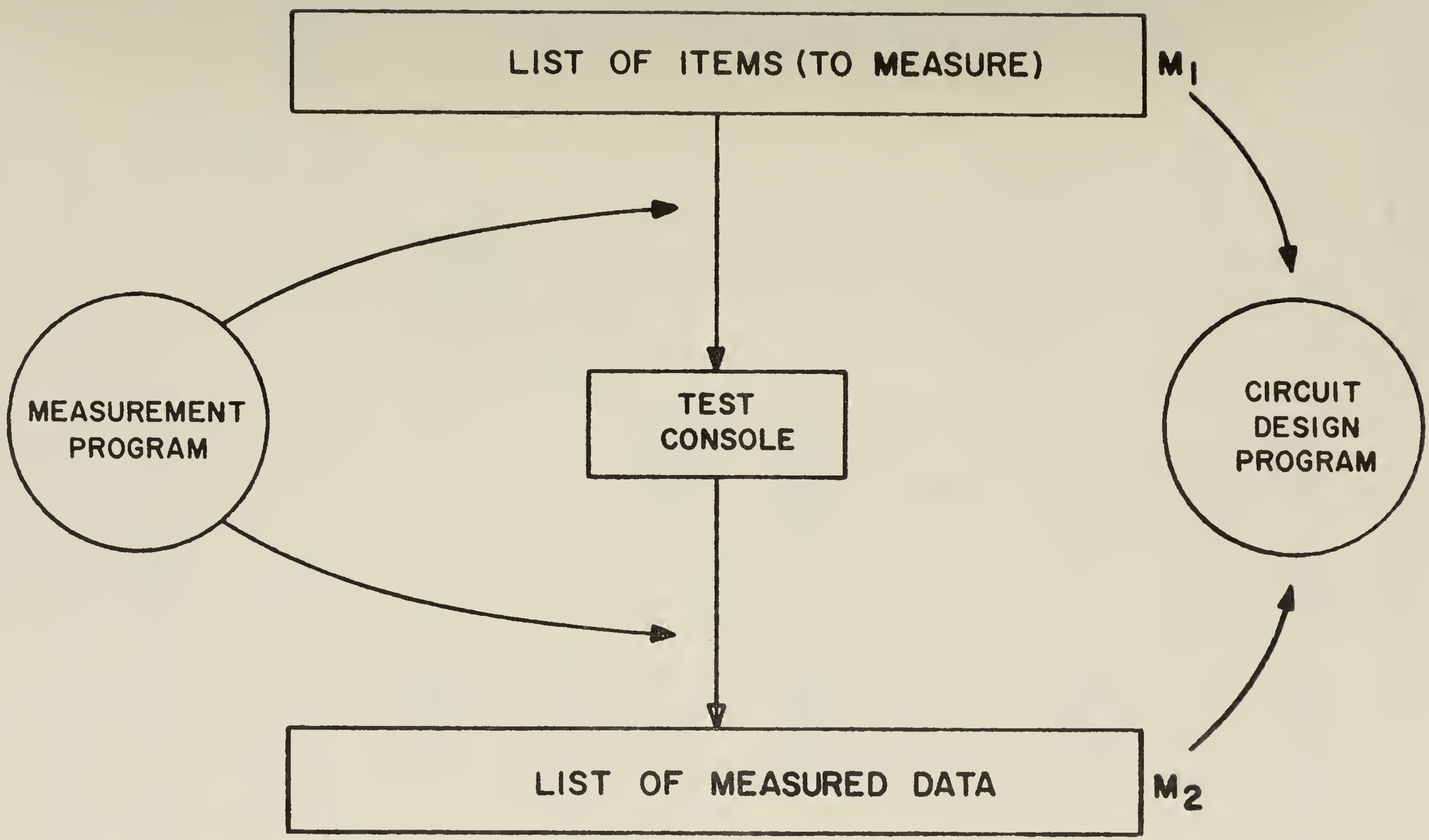
The machine is composed of three main units: Control Unit, Digital Readout Unit, and the Switch Group. The switch group interconnects the digital readout unit with test element and test register. It also specifies the connection between this register and the voltage and current control networks.

Data from the computer describing measurement items and measurement conditions are first read into the Buffer Register. This data is then transmitted to corresponding portions of the Relay Register upon receipt of a control signal decoded from the instruction part of input word. The contents of the Relay Register then dictate the connection mode of the switch group. These switches in turn specify measurement conditions and the input/output connection mode between the digital read scope and test unit. Other switches specify the external programming signal which controls the digital readout scope.

Measured data from the digital readout scope is placed first in the Buffer Register. It is then read out on command from the main computer into a memory bank of the computer.

Data can also be read into the Buffer Register and manually processed step by step. Push buttons are provided at the console for this purpose. This mode of operation is called "pseudo manual operation." Of course, if completely manual operation is desired, the test console need not be on-line to the computer.

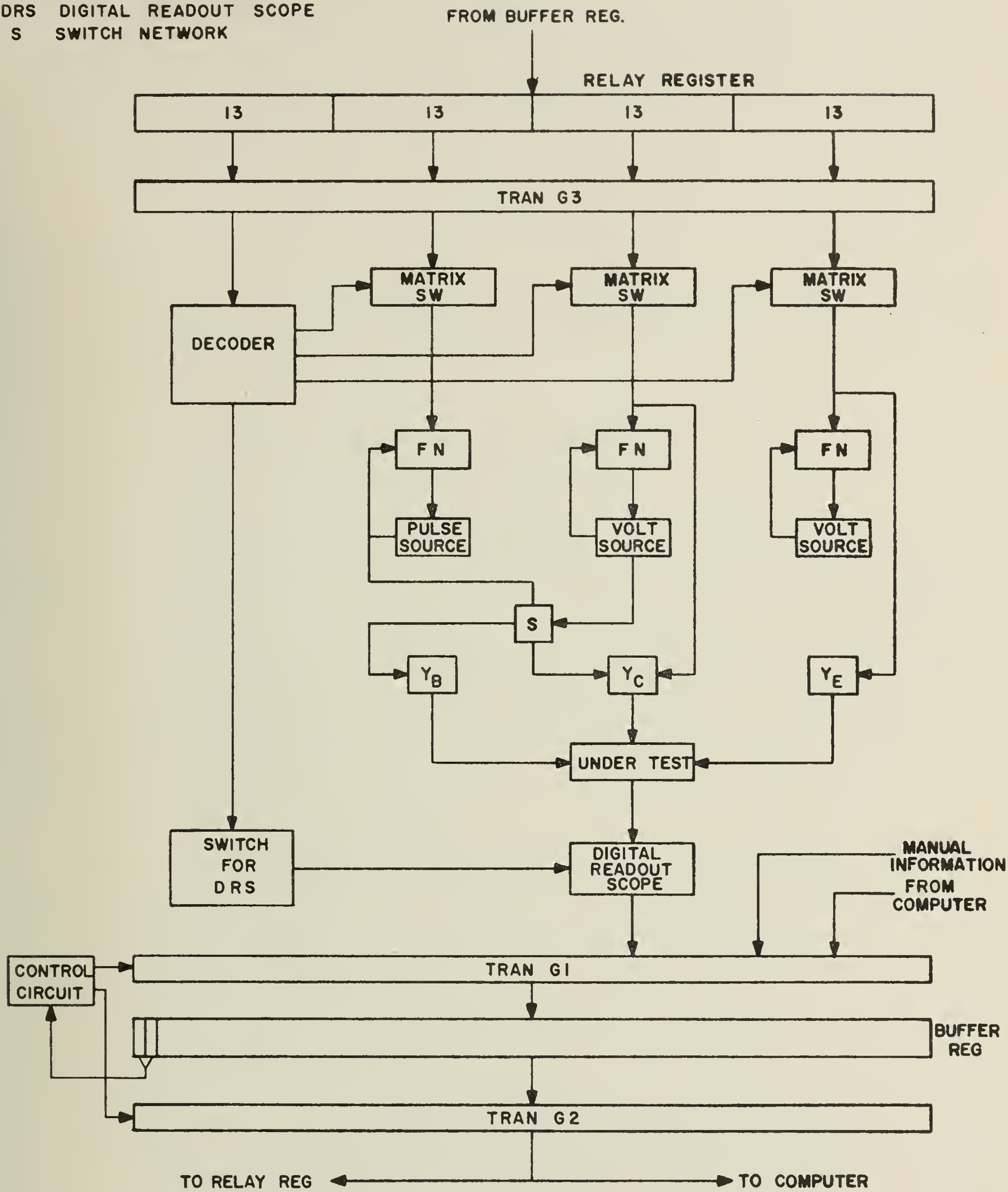
Input and output devices (typewriters, paper tape, etc.) are planned for ILLIAC III and therefore will be available at the test console. Therefore input and output data are fed to the ILLIAC II computer by means of these shared I/O devices.



DATA FLOW THROUGH THE TEST CONSOLE

FIGURE 1(a)

TRAN G3 : TRANSMISSION GATE 3
TRAN G1 : " GATE 1
TRAN G2 : " GATE 2
FN FEEDBACK NETWORK
DRS DIGITAL READOUT SCOPE
S SWITCH NETWORK



REGISTERS & DATA PATHS FOR TEST CONSOLE

FIGURE 1 (b)

1.2 Applications of the Test Console

The machine is capable of all dc and transient measurements required for the selection of transistors, diodes, evaluation of basic printed-circuit board logic circuits (flipflops, etc.) and the development of memory systems. However, it would be necessary to supply additional circuits to evaluate magnetic thin-film circuitry.

1.3 Word Format

Prior to a detailed description of the operation of the Test Console, it is convenient to state the word format used. One word is split into four parts, each part containing 13 bits.

The first 13-bit group indicates the measurement items and the instruction: measure, load, indicate zero error, etc.

The second 13 bits are divided into three groups. The first three bits specify the terminal conditions at the emitter; the remaining two groups describe the units and the decimal point for base and collector terminal conditions.

The third and fourth 13-bit groups give the base terminal condition and collector terminal conditions respectively. If either the base or collector condition need not be specified, one loads the same condition into both the base terminal condition and the collector terminal condition.

Word format is given in Fig. 2.

The item part specifies the appropriate connection mode between the digital readout scope and element to be tested. Connections specified are:

1) connection between the power supply and pulse generator feeding the test element.

2) input connection and channel selection to the digital readout scope (DRS).

3) external programming of the DRS, for example: AMPLITUDE, TIME, PERCENTAGE, SLOPE, MEASURE, and DIFFERENTIAL readout selection.

4) connection between Relay Register and the Y and Y_V networks (shown in Fig. 7 and Fig. 9).

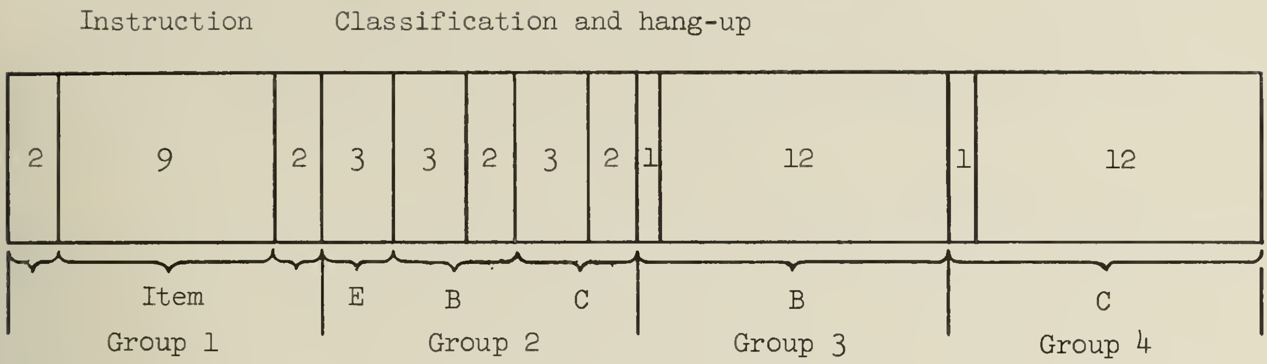


Figure 2. Word Format

Group 1: instruction (2 bits), item (9 bits), and classification (2 bits).

Group 2: first 3 bits specify emitter terminal condition, 5 bits in B and C are for the units (3 bits) and decimal number (2 bits).

Group 3: 12 bits indicate 3 decimal numbers of base terminal condition or, for the case of a logic test, the input circuit condition.
Sign (1 bit).

Group 4: 12 bits indicate 3 decimal numbers of collector terminal condition, or, for the case of a logic test, the output circuit condition.
Sign (1 bit).

1.4 <u>General Description of Operation</u>

Data flow between the test console and the computer is controlled by the computer program, as well as by auxiliary data supplied over the input device (e.g., typewriter). Once data is sent to the Test Console, it controls the operation of the console as discussed above.

Operation of the console can be split into two operating cycles: a "setting cycle" and a "measuring cycle." In the setting cycle, all measurement conditions and connection mode settings are set up. In this machine, all condition settings are carried out by digital feedback to insure high accuracy and stability. The flow diagram of this setting cycle is shown in Fig. 3. Upon completion of the setting cycle, the machine is ready to measure a specified item.

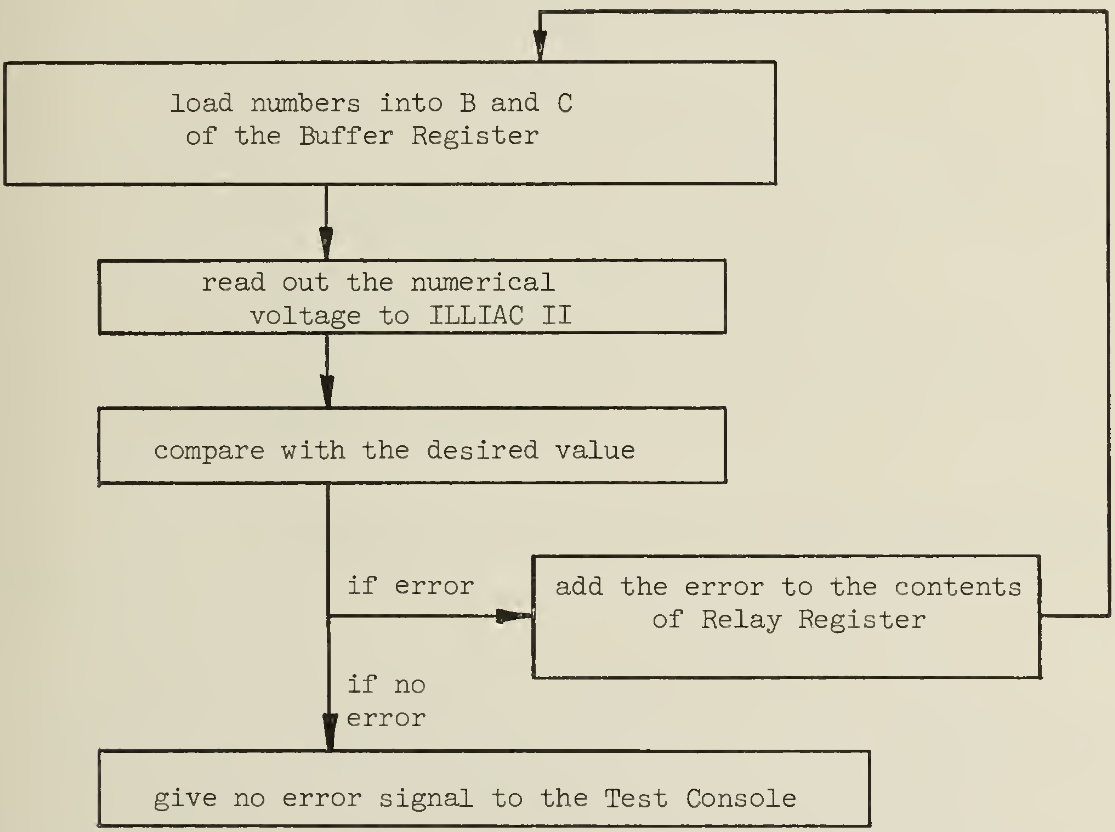


Figure 3. Flow Diagram of the Setting Cycle

Before going into more detail, we give the function of all control signals in Table 1.

TABLE 1. SEQUENCE CONTROL REGISTERS OF THE TEST CONSOLE AND RELATED CHANNEL CONTROL SIGNALS

D FF	give sync signal to interplay channel control
S FF	execute test console set cycle
R FF	execute test console read cycle
S_1 FF	execute test console base condition set
S_2 FF	execute test console collector condition set
DBY FF	tell the computer the test console is or is not ready to communicate
Channel FF	tell the test console which channel is to be read out
Start/Stop FF	connected to the DBY FF and controls the transmission of information
SET	indicates that the channel is occupied
BDI	indicates whether output or input to the computer
GO	signals transmit data
DBY	
SYNC, SYNR	synchronization of the successive data transmissions

In actual practice the setting cycle has two loops, corresponding respectively to setting the base terminal condition (or input network conditions for logic circuit test) and to setting the collector terminal condition (or output network conditions for logic circuit test). For the emitter terminal condition, we do not use a closed loop conditioning control for reasons of economy; the emitter terminal condition is set by selecting one of the available built-in conditions.

After these terminal conditions have been set, the Relay Register will keep these conditions constant during the measurement period, and the machine proceeds to the measurement cycle. (See Fig. 4).

At the end of the measurement cycle, ILLIAC II normally transmits the results to the I/O unit and proceeds to the next subprogram. However, the interplay channel control progress will be interrupted by a "DBY" signal from the Test Console until the start/stop control sets BDY off. This situation is different for Mode 1 operation and Mode 2 operation:

<u>Operating Mode 1 (Multiple Measurement)</u>

In this mode measurement continues until finishing a specified number of measurement for each test piece.

<u>Operating Mode 2 (Single Measurement)</u>

In this mode only one type of measurement is assigned for each test piece.

In both modes, the start/stop key resets the BDY flipflop: at the end of multiple measurement in Mode 1 or at the end of each measurement in Mode 2. Selection of Mode 1 and Mode 2 is determined by programming.

After each measurement, if the control* signal is still on (i.e., Mode 1 operation), the machine is automatically ready to receive or give bits of information. If this signal is off, however, the machine is not ready to receive (give) information from (to) the computer until the start/stop key resets the DBY flipflop to off. This procedure provides for the time interval within which the test piece is being replaced by a new piece.

Measurement control information and an appropriate program are loaded into the computer prior to the start of a measurement. After the data have been transferred to the machine, the set cycle operates as follows: data is decoded. If the data is a positive number, the machine proceeds to the setting of the given terminal condition. After the termination of the setting cycle (the setting cycle terminates when the machine receives the zero error signal from the computer), the Test Console initiates the measurement cycle, and then the readout cycle. Data takeout is controlled by the computer. ILLIAC II can transfer, if desired, the measured results to the output device. Also, a three range classification can be read visually from colored indicator lights on the scope. Finally, the data can be statistically analyzed, etc., by the computer.

*May be sent through special register.

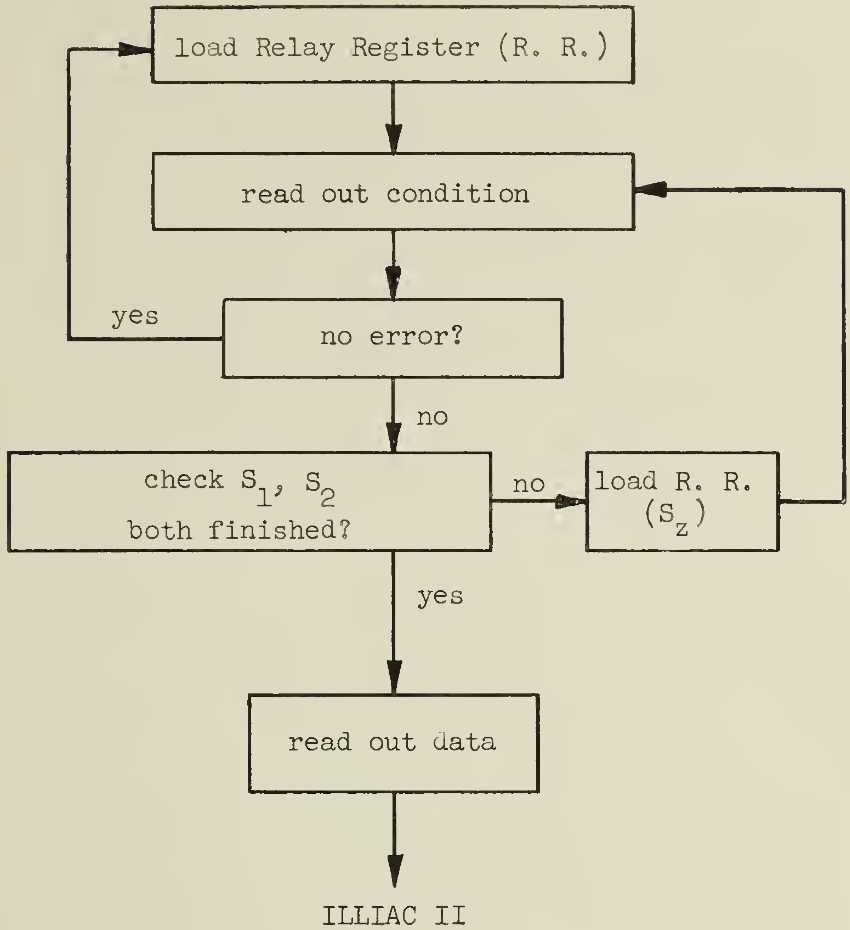


Figure 4. Flow Diagram of the Measuring Cycle

1.5 Manual Operation

Manual operation is carried out by setting the MAN and COMP key to MAN.

For manual operation:

1. Input signals are given by push-buttons at the console.
2. Output signal (measured data) is displayed on the digital readout scope.
3. Classification (low, ok, high) is displayed on the readout scope.

4. Data measurement conditions are given to each E, B, and C section by three coded decimal digits.

5. Readout:

   a. Digital number, unit, and decimal point specifying base setting conditions are read out into the B portion of the Buffer Register.

   b. Digital number, unit, and decimal point specifying collector setting conditions are read out into the C portion of the Buffer Register.

   c. The measured data is read into the B and C portions of the Buffer Register, and transmitted from there to the high-speed register of the computer.

In each setting cycle the measurement instruction with a revised input value (initial setting number plus error) must be loaded into the Buffer Register of the machine until the Zero Error signal is sent to the Test Console. Accordingly, each time S FF is set by the instruction.

The Zero Error signal might be sent to the machine either through the special path from the computer or as data through the interplay information channel. In the present situation, Zero Error signal is indicated in the instruction part of the data from the interplay (instruction part is 00 in this case). The Zero Error signal resets the S_1 flipflop, which indicates that the machine is in the base setting cycle, and therefore sets R FF. The setting cycle then proceeds automatically to the next setting cycle--if the S_2 flipflop is in the set state. After R FF is set by the Zero Error signal, "DBY" changes to "1" to inform ILLIAC II that the machine is busy.

When R FF is set, the gates GIR(C)G which connect the readout information to the collector portion in the Buffer Register are ready to transfer the readout data. At the Read Command signal from the control unit (following the Measurement End signal from the DRS), the measured data are transferred to the Buffer Register. After the completion of this data transfer, the R FF is reset by the Read End signal, and the DBY changes to "0" indicating that the device is not busy. The SET signal from Interplay resets DBY to "1," and the measured data in the Buffer Register is transferred to the computer by opening the gate G2GC in conjunction with the BDI and GO signals from Interplay.

1.6 Channel Selection

We have two output channels which must be connected to the computer in the set cycle because the setting error must be added to the contents of the Relay Register. This channel selection is accomplished by the machine automatically without any specific instruction in the data from Interplay.

The first readout in the set cycle always transfers data from the Buffer Register; the second readout in the set cycle always transfers the data from the Relay Register. Then the measured data is transferred from the Buffer Register. These two readout channels are controlled by the content of the channel FF, which changes state cyclically under control of the signal BDI $\cap$ SET. The table of channel selection is as follows:

	Channel FF
First readout in set cycle	1
Second readout in set cycle	0
Data Read readout	1
First readout for manual operation	0

If both S_1 and S_2 are zero, the channel FF does not change state.

1.7 Pseudo-Manual Operation

In this operating mode all measurement conditions and measurement items are specified by pushing buttons on the console. Setting conditions are adjusted by the program to the correct value, and the measured data is displayed on the digital readout unit. The readout number is displayed until the reset occurs prior to proceeding to another measurement. The sequence is as follows:

1. Turn the MAN-COMP key to the MAN side 2. Push DATA button and ITEM button 3. Select E, B, C button 4. Push SET button	conditions and items are loaded into the Buffer Register. DBY FF is set to "1."
5. Push READ button	loads the Relay Register, connections between DRS and test piece are completed.
6. Operate START/STOP key	DBY FF returns to "0"-- new control signals are transferred from computer to the test console.

The program which allows communication between the machine and the computer must be loaded into the computer before proceeding to the measurement. The loaded program in the computer remains in the input state until the DBY FF turns to "0."

Once the control signal is transferred to the machine, subsequent operation of the test console is the same as for automatic operation. Therefore, G1C is controlled by the S_1 and S_2 signal to allow information transfer from the computer, even in manual operation. This situation comes from the feedback control of the setting condition.

The Channel FF is set to "1" by the MAN $\cap$ READ signal from the console to read out information from the Relay Register. The READ button loads the instruction bit into the Buffer Register. G2R(B), G2R(C), and G2R allow information to transfer to the Relay Register from the Buffer Register. After the information has been transferred to the Relay Register, the Local Set End signal disconnects G2R.

1.8 Display Time Control

When the R FF is set and Measure End signal is on (Pin GG on the rear of the 6R1 digital readout unit reads +20 volts when it is on), pin HH of the 6R1 is connected to ground. During the period in which HH is connected to ground, the 6R1 unit stores the measured data in its decade counter. Therefore, HH is connected to the ground by the signal R FF $\cap$ GG, and disconnected by the Read End signal in ordinary operation. But in manual operation, the readout number is given by the display on the 6R1. Therefore, until the operator recognizes the measured number on the display, the signal $\overline{S}_1 \cap \overline{S}_2 \cap M$ inhibits the decade counter reset until the next operation of the START/STOP key resets the R FF.

1.9 Successive Manual Operation

In successive manual operation, the same measurement condition and the same measurement items are successively processed for each test piece. Therefore, the condition setting cycle need not be repeated after the first test. Only the START/STOP key need be operated after inserting each new test piece.

This is accomplished in the following way: Once the conditions are set up in the Buffer Register for the first test, the instruction bit in the

Relay Register is set to "1," and the contents of the Relay Register are the same as the contents in the Buffer Register. Since the first readout is from the Relay Register, as described before, the measurement conditions are loaded into the memory of the computer. Then follows the setting program shown in Fig. 3. The instruction bit is not tested. Now, by the readout program, which follows the setting program, the contents of the Buffer Register are transferred to the computer and the instruction bit tested. All data from the Buffer Register has "0" in the instruction bit. Therefore, by the program in Fig. 5, the process does not go back to the loading program but goes instead to the measurement program--unless the SET and READ buttons are operated again.

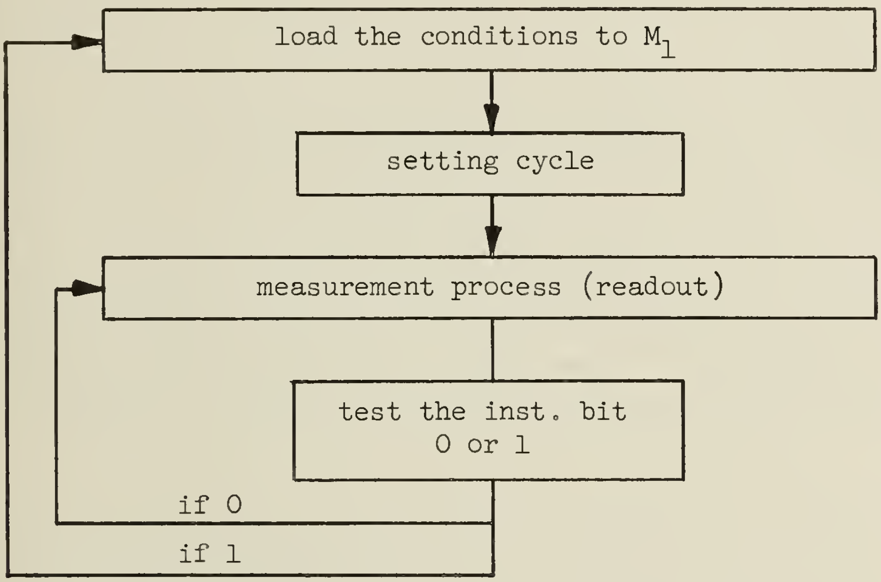


Figure 5

1.10 Manual Operation without Connection to the Computer

For manual operations every step is executed manually. No communication occurs between the machine and the computer. The internal-external program control switch of the 6R1 unit is switched to the internal program side. All conditions and items are specified at the console. Automatic feedback control is not available as for ordinary measurements.

Data push-buttons provide very close ($\pm$ one per cent) control of the supply voltage and the pulse generator voltage without any external feedback device. The S FF and R FF are set automatically by pushing the ITEM and

SET and READ buttons on the console. By pushing these buttons, the test piece is connected correctly to the input of the DRS, and the measurement conditions are stored in the Relay Register.

The major difference between pseudo-manual operation and manual operation is the absence of feedback control in the latter case. Therefore all setting conditions must be controlled manually. Manual control is important in the present situation because the DRS cannot be programmed completely by an external program. All the controls of amplitude and of sweep velocity must be adjusted by watching waveforms on the scope.

Therefore, the control of the units, that is, in amplitude, time, and mode selection of the sweep unit, is not programmable externally. These are important parameters for the condition setting because the comparison in the setting cycle must be made when the readout data and the given condition have similar units.

Until the DRS can be programmed externally for the above parameters, we must check manually whether the readout data has the same unit as the given conditioning value. When measuring current, we must select the differential readout mode. The digital readout value is determined from the display on the sampling scope in every case, and if the display is over-scaled the digital readout will not show the correct value. Hence, prior to automatic measurement, we must adjust the sweep velocity and amplitude on the scope to get a correct readout.

These characteristics of DRS make it impractical at the present time to have a completely programmed operation, but the control circuits of the machine provide the possibility of complete external programming upon a future modification of the digital readout scope.

1.11 Automatic Operation

This operation is the same as the psuedo-manual operation except for a difference in the condition setting procedure. (For pseudo manual operation, conditions are set manually.)

The operating program starts from the OUTPUT order to the Test Console. All measurement conditions and items are specified by the computer program prior to the actual measurement. In the same way as for pseudo-manual operation

(shown in Fig. 5), the same kind of measurements can be made on the successive test pieces by merely operating the START/STOP key at the beginning of each measurement. To change measurement items, one replaces the former item by requesting new items through the input device (typewriter, etc.), or, as in the case of pseudo-manual operation, feeding the new item into the Buffer Register.

The second mode of operation, which allows successive measurements for each test piece, is carried out as follows:

1) Load a list of the successive measurement items into the memory M_1 in the computer;

2) Set the number N (the numbers of measurements) in a special counter in the computer and proceed with the following program (Fig. 6):

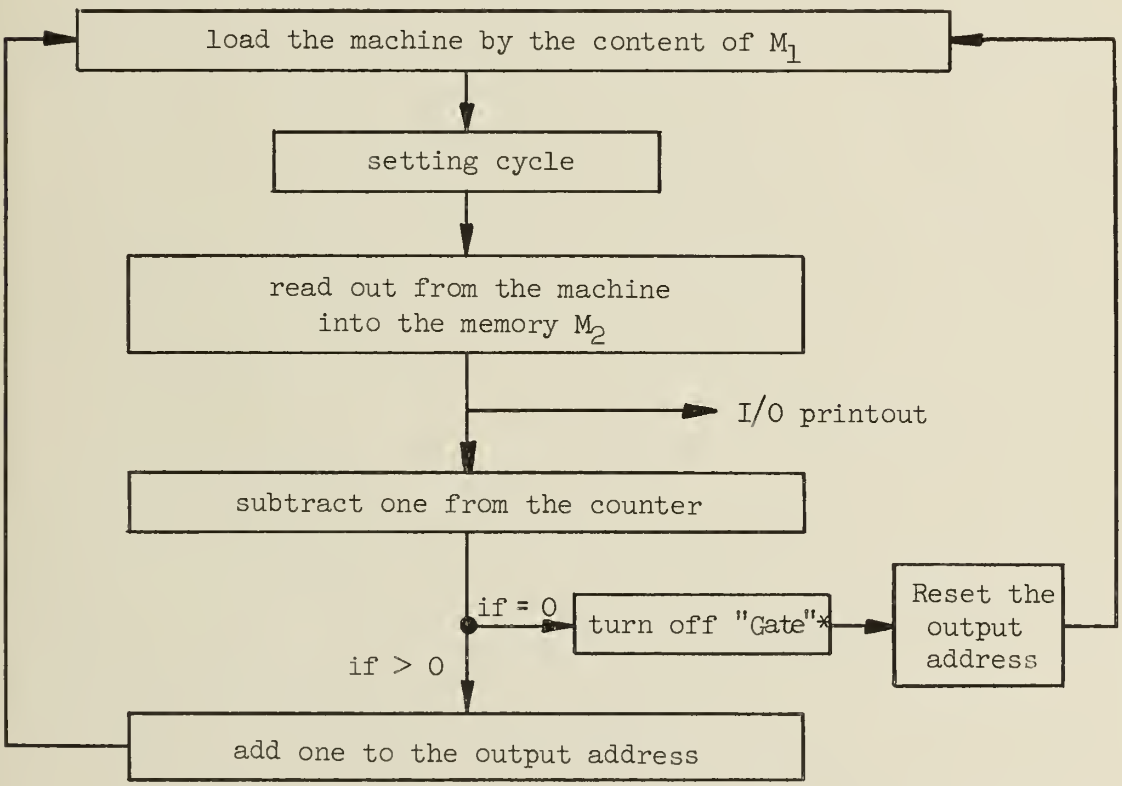


Figure 6

*The same kind of control gate signal described on page 8.

In the Test Console if GO from the Interplay changes (turns to "0"), the DBY FF is reset at once, but after a short delay this again is set, and remains in this state until the next operation of the START/STOP key.

Readout data is stored in the memory of the computer and used in the following applications:

1. data analysis and other programming.

2. transferred to the output device(s) and printed out.

3. compared with a reference value table for classification, and the Test Console informed of the classified level by the special bit (10th, 11th, 12th bit), or this classification printed out with the data.

2. ENGINEERING DESIGN

2.1 Basic Units of the Test Console

There are six basic units in this machine. They are:

1. Control networks for the power supplies and pulse generators.
2. Control networks for external programming of the Digital Readout Scope (DRS).
3. Console registers.
4. Buffer and Relay Registers.
5. Control and decoding circuits of the machine sequence control.
6. Cable drivers and terminators of the ILLIAC II/Test Console interplay channel.

2.2 Control Networks (Y_v) for Supply Voltage Selection

All control of supply sources is accomplished digitally by means of the Relay Register and the Relay Networks. The Relay Networks are shown in Fig. 7, each contact a_i is shunted by a resistor. These resistors are arranged to give three coded decimal numbers.

The constant current through the remote sensing resistance of the Kepco power supply is adjusted at 1 ma for the dc supply voltage and slow pulse generator, and is adjusted at 2 ma for the fast pulse generator. Either the slow pulse generator or the fast pulse generator is connected to the base terminal, depending on whether it is a time measurement or a dc measurement. When the fast pulse generator is connected, the resistance value of the control circuit of Kepco supply is changed by the relay to give a more sensitive control (normal sensitivity is 1 volt/KΩ) and a high output voltage (in fact, of twice the magnitude because the pulse out of the type 110 pulse generator is exactly one-half of the external supply voltage).

2.3 Unit Selection and Decimal Value Control

Units and decimal value for base and collector terminal conditions are given in one quarter word and transmitted to the machine either manually or by

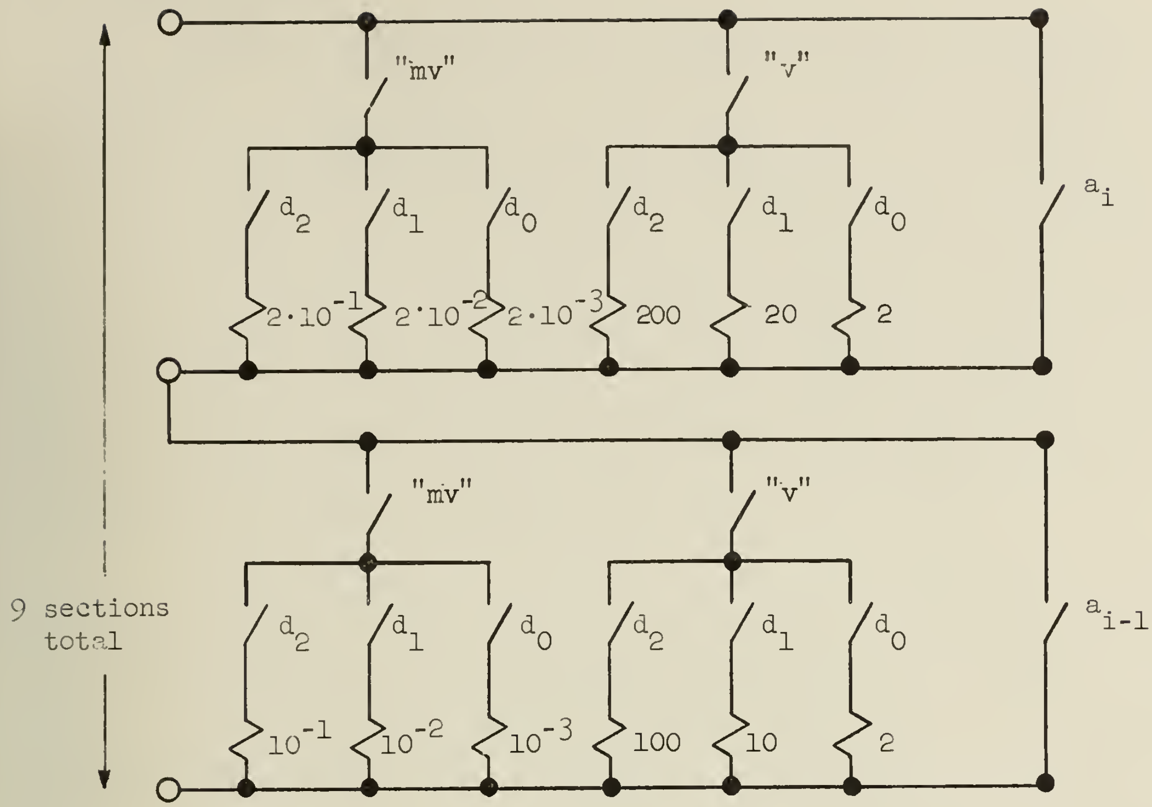


Figure 7. Relay Networks for Digital Control of Supply Sources

the computer program. The machine can handle two units of voltage (v, mv) and two of current (μa, ma).

For each unit, a three-decimal-digit number is assigned. Each decimal digit is encoded in binary form with each binary digit corresponding to one a_i contact in Fig. 7. Each resistance which is shunted by an a_i contact separates into two paths: one corresponds to the unit "v" and the other corresponds to "mv." In each path resistance value is weighed in a decimal manner:

$$Z = \left(d_0 Z_0 + \frac{d_1}{10} Z_0 + \frac{d_2}{100} Z_0\right) a_0 + \left(d_0 Z_0 + \frac{d_1}{10} Z_0 + \frac{d_2}{100} Z_0\right) 2^{-1} \cdot a_1 + \ldots$$

The decimal point decoder output selects either d_0, d_1 or d_2. These contacts are made in parallel by CR12Z reed relays driven by a 2N1530 npn silicon transistor.

2.4 Current Setting

A current setting for given units (ma or μa) is accomplished in the following way: the voltage across terminals of a special network (Y), serially inserted in Y_v, is measured. One of the terminals of Y is connected to the A channel of the DRS and the other terminal is connected to the B channel of the DRS, and the mode switch A + B is selected. Now, when the current is specified to be i ma, for instance, the decimal number i is read into the Y_v network, and the unit (ma) selects the corresponding switch to give the correct range of resistance value. Sometimes, however, we must specify the base or collector load resistance (e.g., diode anode, or cathode, load resistance) as well as the magnitude of the current. In these cases, the resistance value of the Y network is specified by a method to be described later.

The Unit Register is used jointly for both voltage and current unit selection. When the current value is specified, we must give both the voltage value and resistance value in order that the current can reach the specified value. In this situation, the unit and decimal point of the Y_v network and Y network are specified as shown in Table 2. As described before, the numerical value of the current is read into the Y_v network but the unit selects the magnitude of the given current (ma or μa).

TABLE 2. CONTROL OF Y AND Y_v FOR GIVEN CURRENT

a. Units Decoder (for both B and C)

	input			output				
	X_0	X_1	X_2	Y_0	Y_1	Y_2	Y_3	Y_4
mv	0	1	0	0	1	0	0	0
v	0	0	1	0	0	1	0	0
ma	0	1	1	0	0	1	1	0
μa	1	0	0	0	0	1	0	1
KΩ	0	0	0	1	0	0	0	0

b. Decimal Point Decoder for Y_v

input				output		
Y_4	Y_3	X_1'	X_2'	D_1	D_2	D_3
X	X	0	0	0	0	0
X	X	0	1	1	0	0
0	0	1	0	0	1	0
0	1	1	0	1	0	0
0	0	1	1	0	0	1
0	1	1	1	0	1	0
1	X	X	X	0	1	0

Y_1 selects mv switch in Y_v

Y_2 selects v switch in Y_v

Y_3 selects ma switch in Y

Y_4 selects μa switch in Y

Y_0 selects KΩ switch in Y

When the current must be set, the resistance values are specified as shown in Tables 3 and 4.

TABLE 3. DECIMAL POINT DECODER FOR Y

input		output			
X_1'	X_2'	D_0'	D_1'	D_2'	D_3'
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLE 4.

Y_3	Y_4	D_1'	D_2'	D_3'	value of Y	series resistance
1	0	1	0	0	1 K	10 Ω
1	0	0	1	0	0.1 K	1 Ω
1	0	0	0	1	0.1 K	1 Ω
0	1	1	0	0	10 K	10 K
0	1	0	1	0	1 K	1 K
0	1	0	0	1	1 K	1 K
0	0				no selection	
1	1					

It is occasionally necessary to change both the supply voltage and the series resistance, especially for transient measurement. If the Y network represents any two-decimal-digit number, then the appropriate resistance value can be loaded in the RIO by a gate signal G2'R, when the instruction is "LOAD." The RIO prepares two digits of a decimal number to connect Y network resistance, and also to connect Relay in input circuit or output circuit (Fig. 8). The decimal point decoders D and D', and the network are connected as shown in Fig. 9. To load a resistance value, push buttons "L" and "Set" (manually), or give "LOAD" (automatic).

The instruction "LOAD" is also used when loading the input circuit (Fig. 10) and output circuit (Fig. 11) for logic circuit tests.

TABLE 5.

1 0	Load	Load the input and output circuit, load the resistance value. Value is given in the RIO.
0 1	Measure	Measurement condition is given in the Relay Register.
0 0	Zero Error	
1 1	Classify	

2.5 Measurement Item Selection

Measurement items that can be selected have been chosen temporarily as follows:

2.5.1 Time Measurement

Transistor	Diode
storage time	recovery time
delay time	
buildup time	buildup time
fall time	

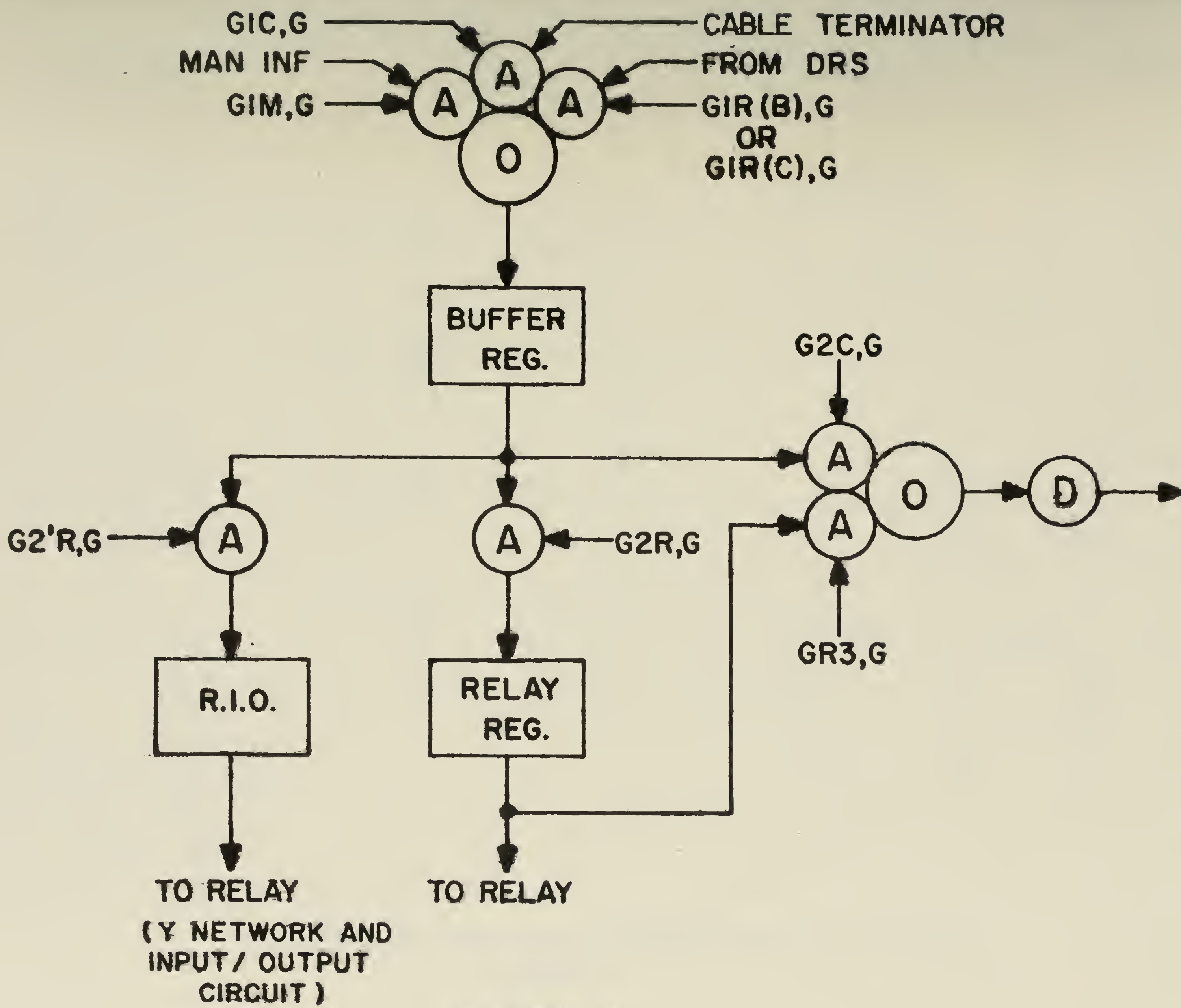
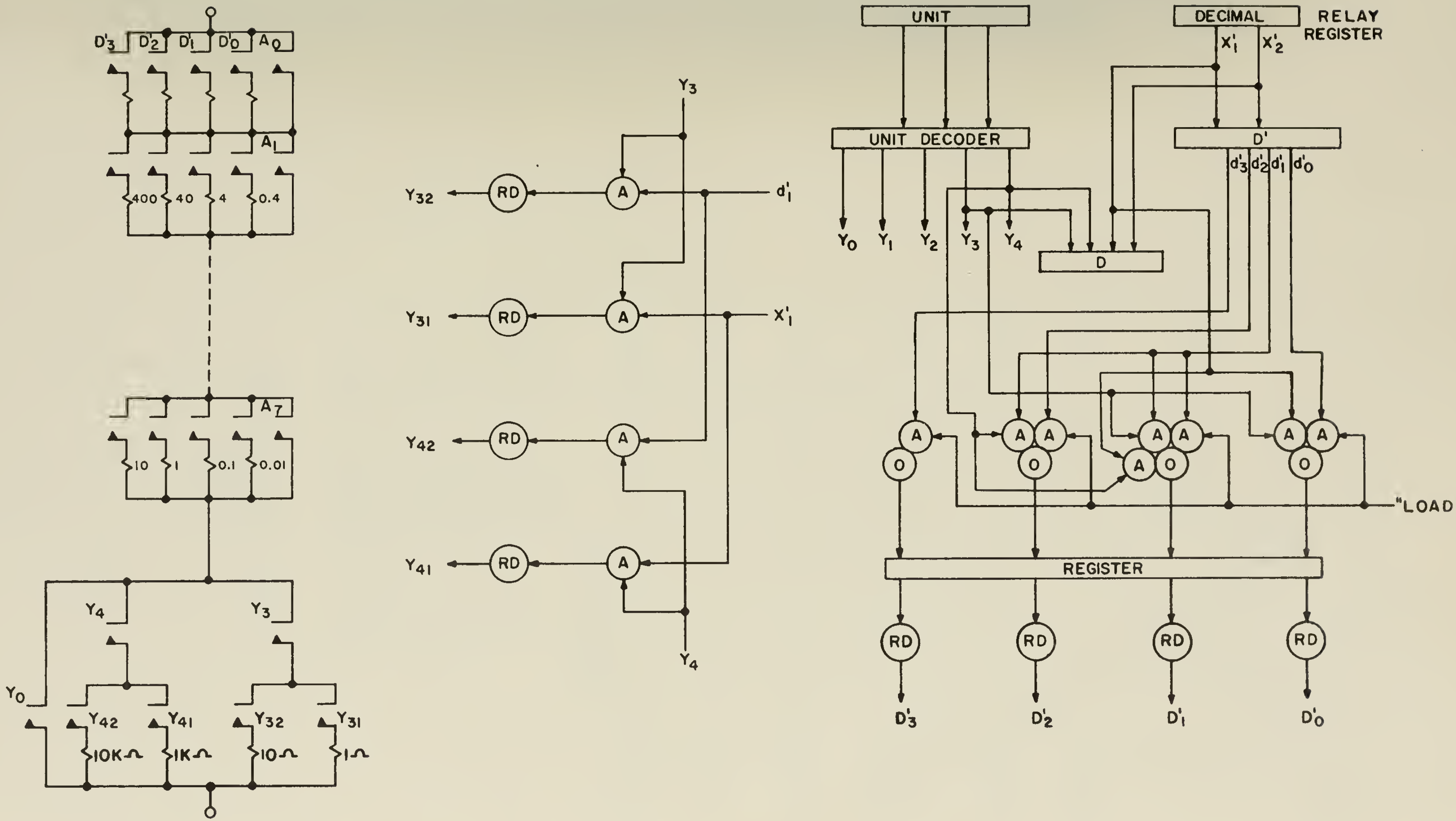
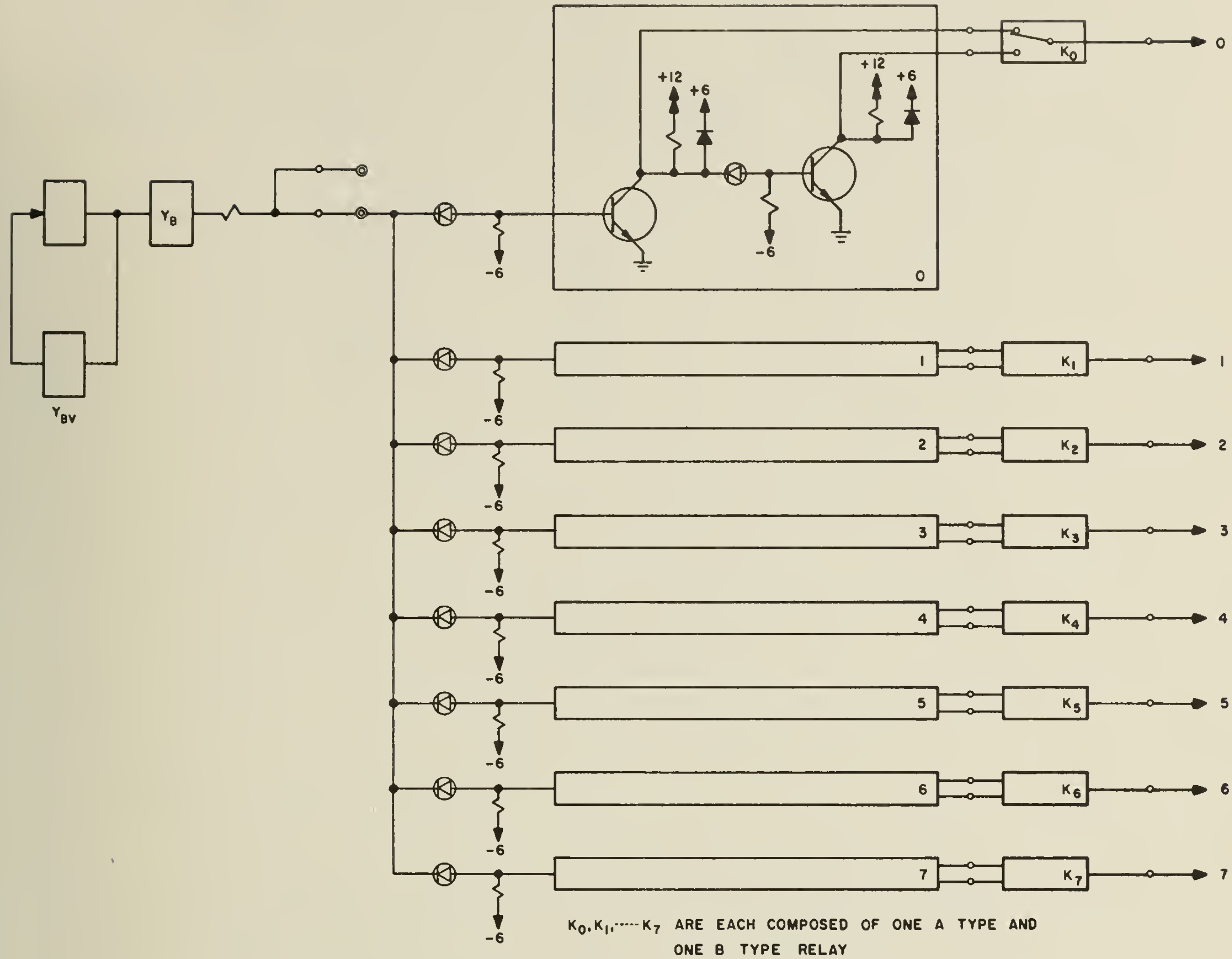

GIC,G
MAN INF
GIM,G
CABLE TERMINATOR
FROM DRS
GIR (B),G
OR
GIR(C),G
A
A
A
O
BUFFER
REG.
G2C,G
A
A
O
D
GR3,G
G2'R,G
A
A
G2R,G
R.I.O.
RELAY
REG.
TO RELAY
(Y NETWORK AND
INPUT/ OUTPUT
CIRCUIT)
TO RELAY

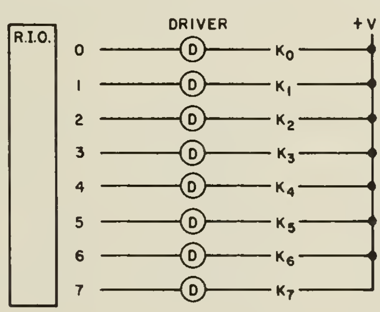
FIGURE 8



CONNECTION OF DECIMAL POINT DECODERS WITH THE Y NETWORK

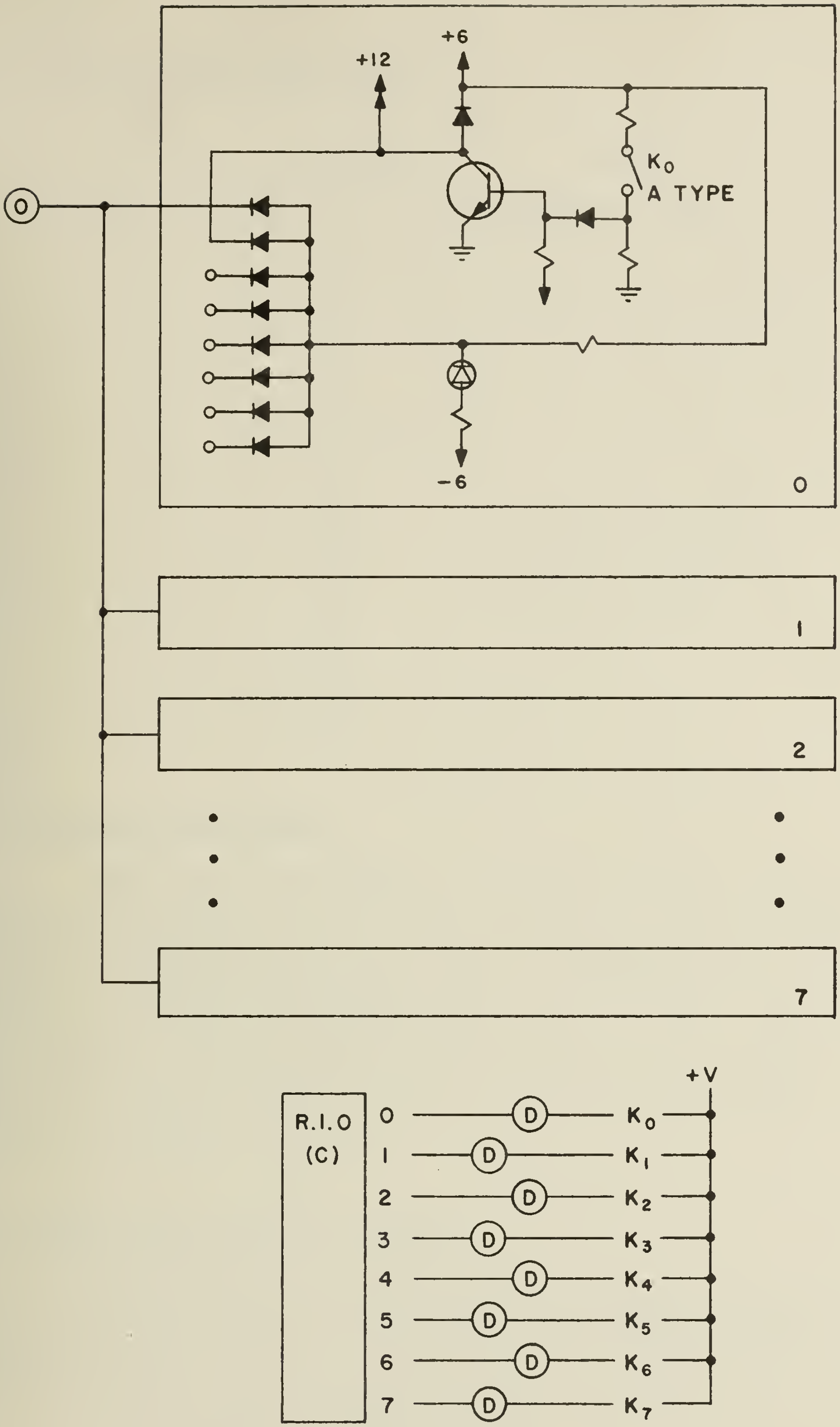
FIGURE 9





LOADING THE INPUT CIRCUIT

FIGURE 10



LOADING THE OUTPUT CIRCUIT

FIGURE 11.

2.5.2 dc (Slow Pulse) Measurement

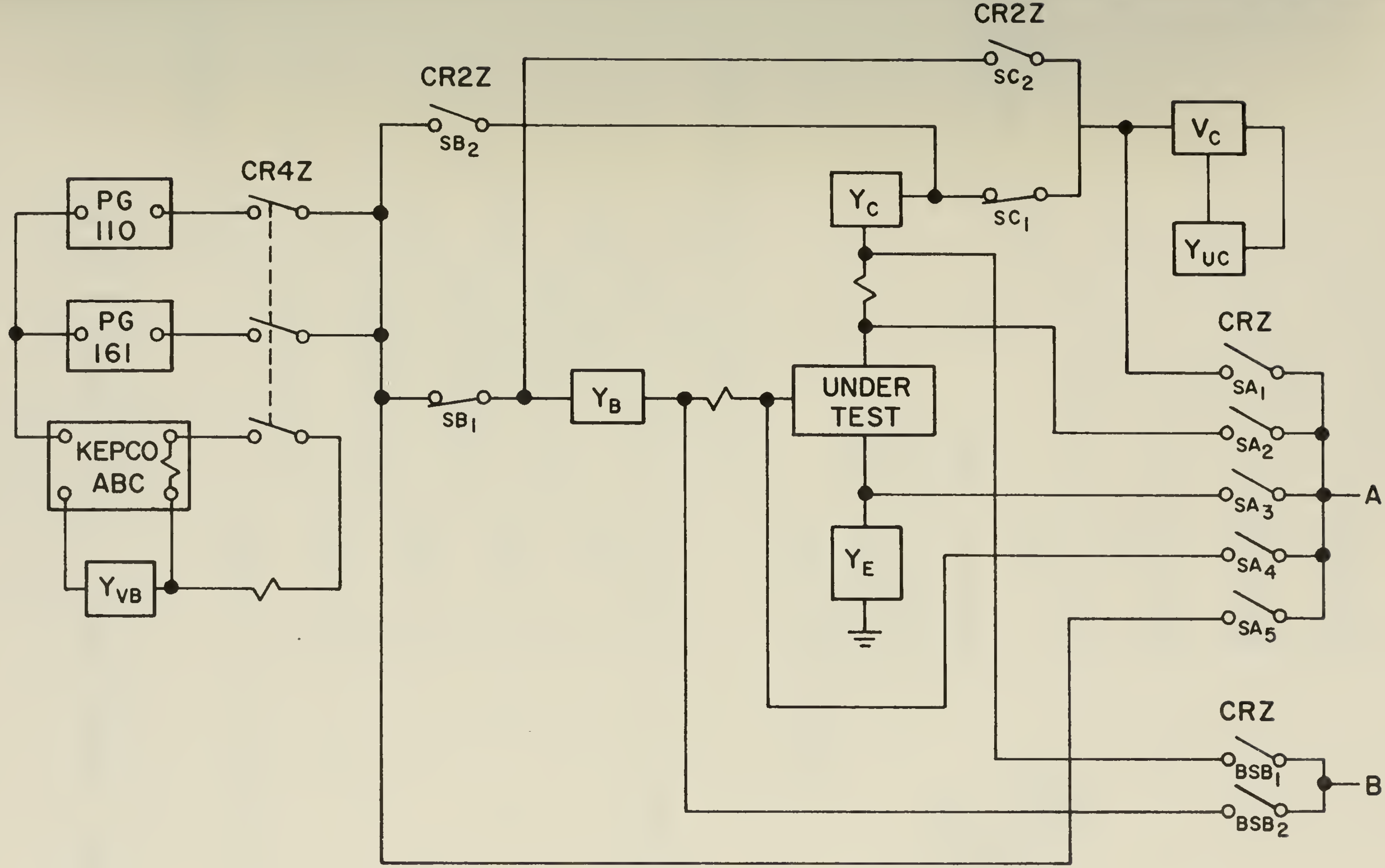
Transistor	Diode
I_{CBO}	leakage current
I_{EBO}	
h_{FE}	
V_{CEO}	
$V_{CE(sat)}$	
V_{CER}	
V_{CBO}	breakdown voltage
V_{BE}	forward voltage
V_{CE}	
V_{EBO}	

2.6 Logic Board Measurement

Logic board measurements are carried out by the same measurement method used to specify the load resistance value. First the LOAD instruction and then the MEASURE instruction is given. Items specified in the Buffer Register are decoded. The decoder output drives a matrix circuit to operate relay contacts: the connection between the DRS, the test piece and supply source (Fig. 12); the per cent network (Fig. 13) and finally the relay network for external programming of the DRS.

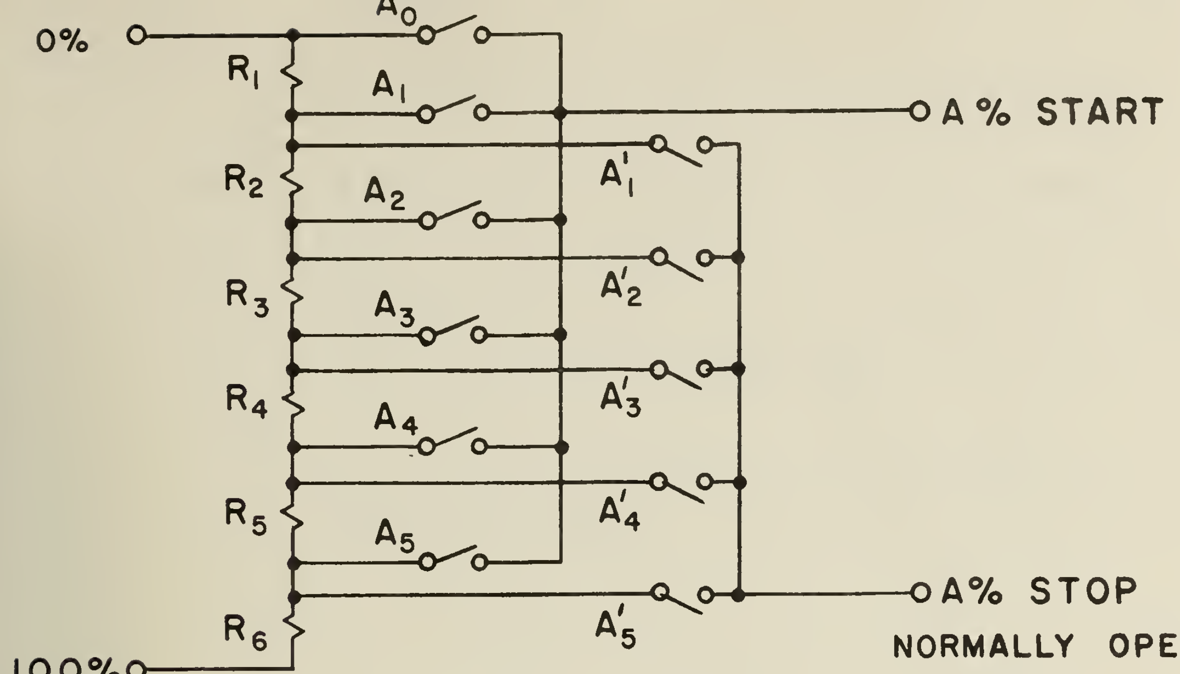
2.7 External Programming of the DRS

For external control of the DRS, selections executed by sensitive reed relays are shown in Table 6. Connections are changed according to the machine operating cycle.



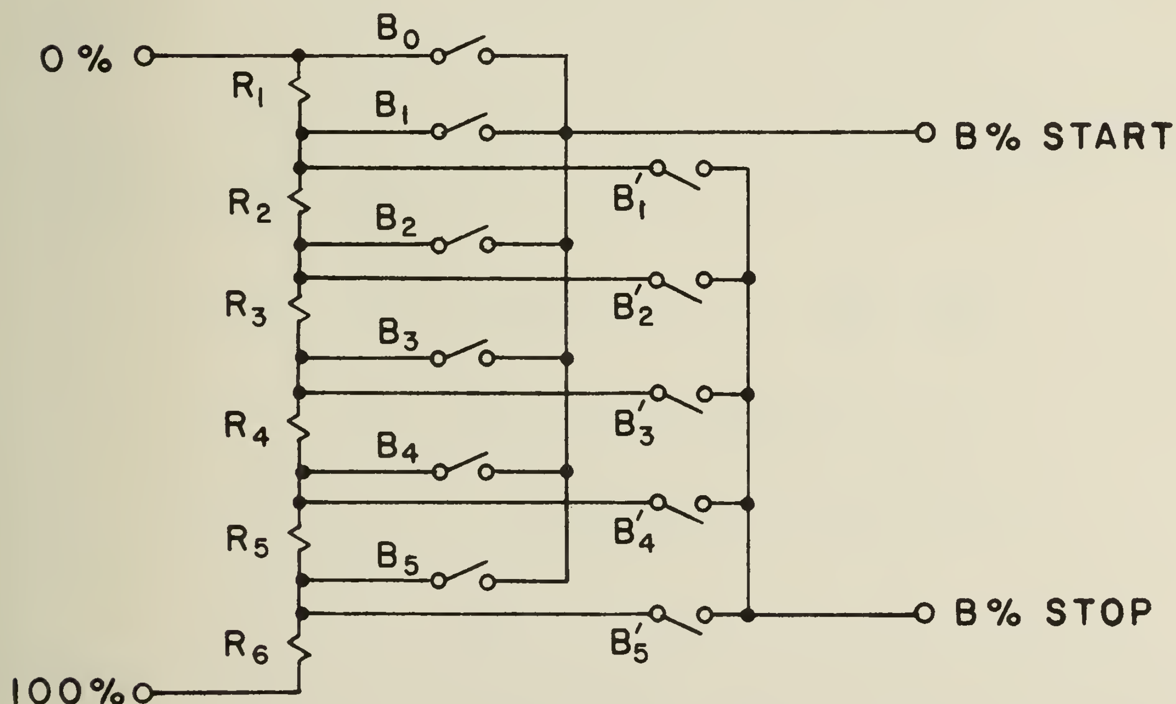
CONNECTION BETWEEN DIGITAL READOUT SCOPE, TEST PIECE AND SUPPLY SOURCE

FIGURE 12



NORMALLY OPEN
RELAY
125.0 K (TOTAL)

10% R_1 = 12.5 K
20% R_2 = 12.5 K
50% R_3 = 37.5 K
70% R_4 = 50.5 K
R_5 = TRM = 12.5 K



PERCENTAGE OF Y NETWORK SELECTION

FIGURE 13.

TABLE 6. MEASUREMENT SELECTIONS AVAILABLE AT THE DRS

K_1	time measurement or amplitude measurement selection
K_2	starting channel A or B
K_3	starting slope + or -
K_4	select first slope or second slope
K_5, K_6, K_7	these are the stopping controls corresponding to K_2, K_3, K_4 respectively

2.8 Information Loading and Readout

Push-button information is first fed to encoding circuits and then connected to the Buffer Register. Readout data (three decimal numbers, units of measure, and the position of the decimal point) are also fed to the same kind of encoding circuit, and transferred to the Buffer Register (Fig. 14).

Units from the GR1 are M, N, μ, V, S on pins Y, Z, AA, BB, and CC respectively, and the unit push buttons on the console are M, μ, V, A and KΩ respectively. Units from the 6R1 and the push buttonsare decoded prior to feeding them to the encoder. These are:

$$V = BB + V, \quad MV = Y \cap BB + M \cap V$$

$$MA = M \cap A, \quad \mu a = \mu \cap A$$

$$msec = Y \cap CC, \quad \mu sec = AA \cap CC, \quad nsec = Z \cap CC$$

$$K\Omega = K\Omega .$$

The Read command gate actually takes out data from the 6R1 unit (see Fig. 15). The gate G1RG feeds the readout data to the encoder. The momentarily operated push button "SET" transfers the push button information to the encoder. G1M (B) (C) and G1R (B) (C) are the gate signals to transfer manual information and readout information respectively to the Buffer Register, G1M (B) (C) (E) are simply generated by the circuit in Fig. 16.

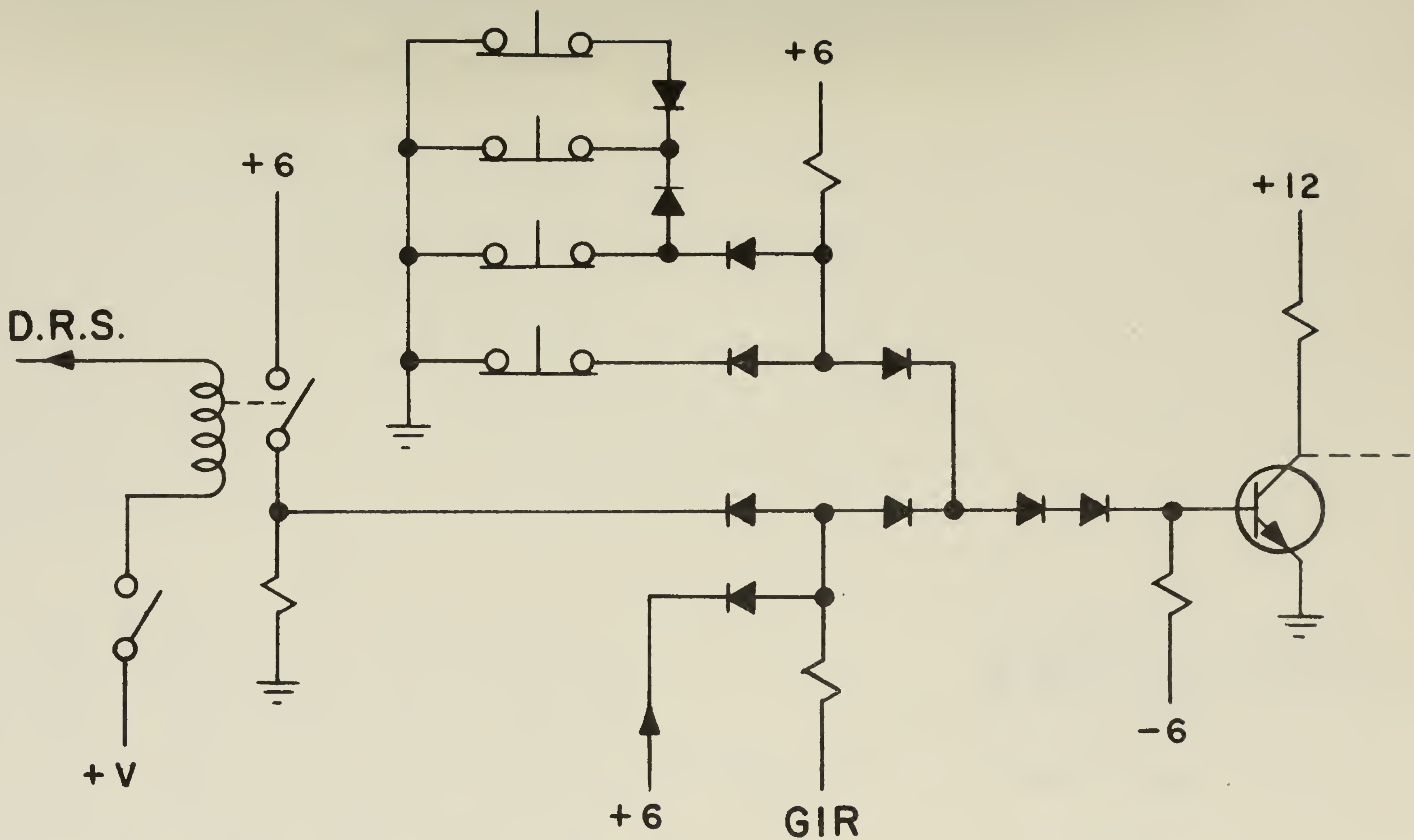
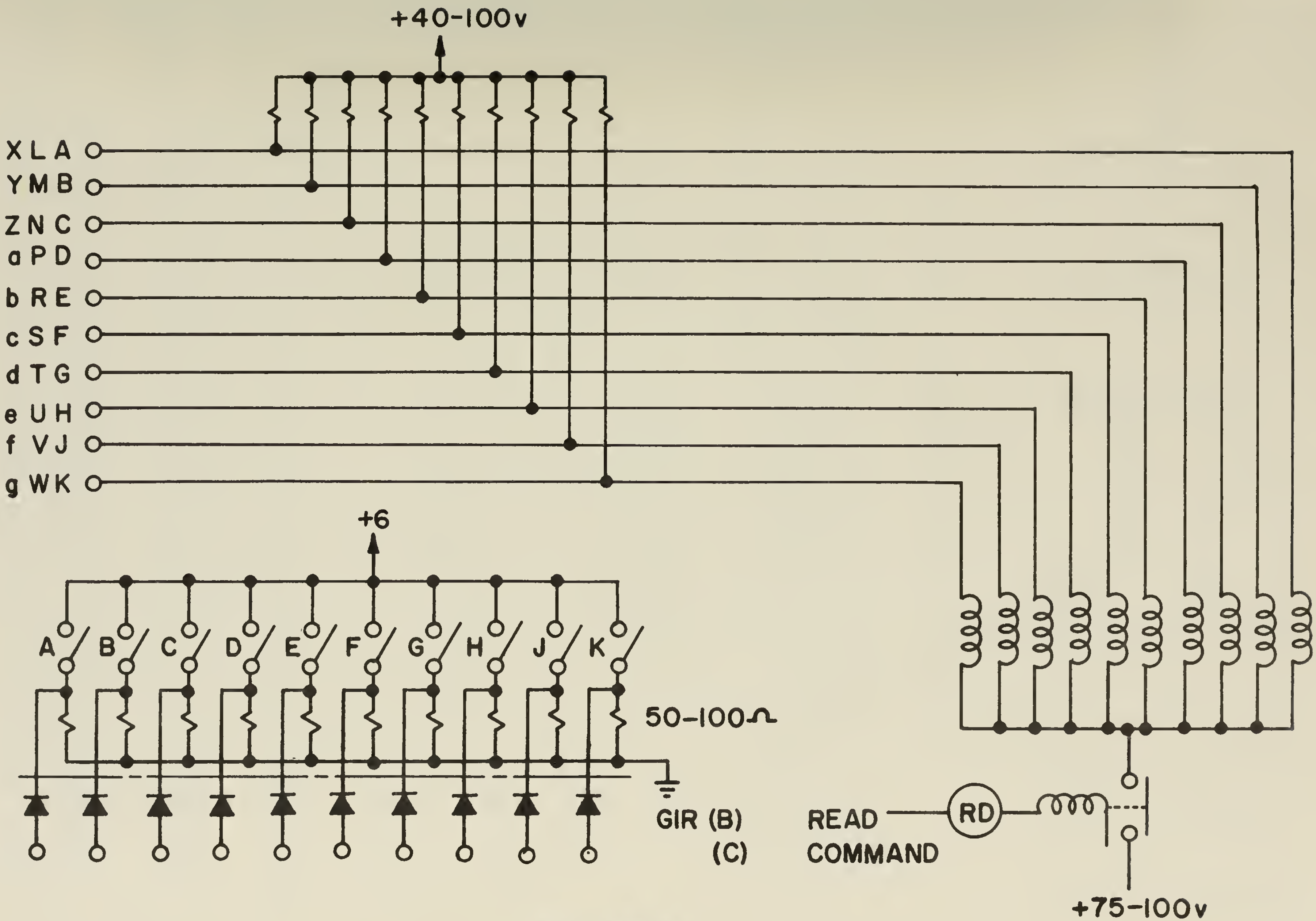


FIGURE 14.



+40-100v
XLA
YMB
ZNC
aPD
bRE
cSF
dTG
eUH
fVJ
gWK
+6
A
B
C
D
E
F
G
H
J
K
50-100Ω
GIR (B)
(C)
READ
COMMAND
RD
+75-100v

FIGURE 15

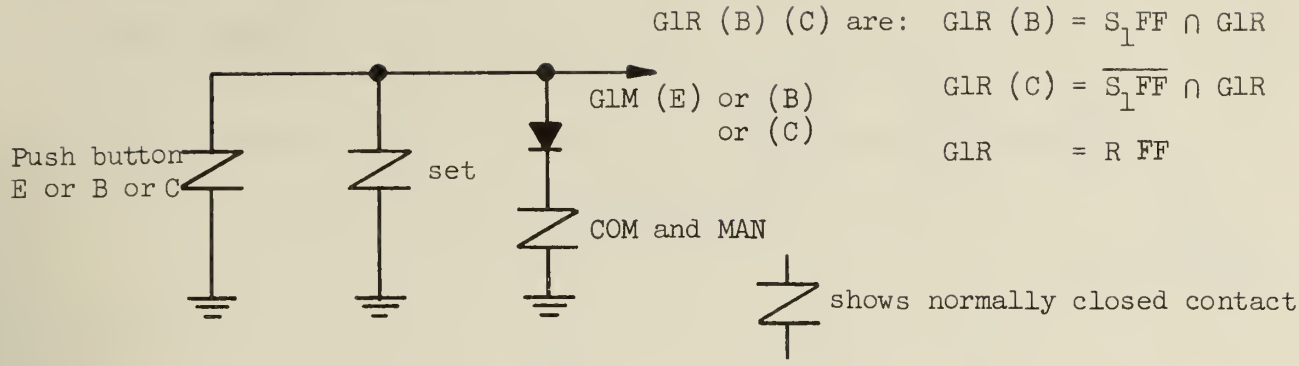


Figure 16. Generation of G1M (B), (C), or (E)

Contents of the Buffer Register are transmitted to the computer by the G2CG, and to the Relay Register by G2RG, G2R (B) G, G2R (C) G, and by G2R'G to the RIO or Y_B (Y_C). Data in the Relay Register is read into the computer by G3CG. These gate signals are:

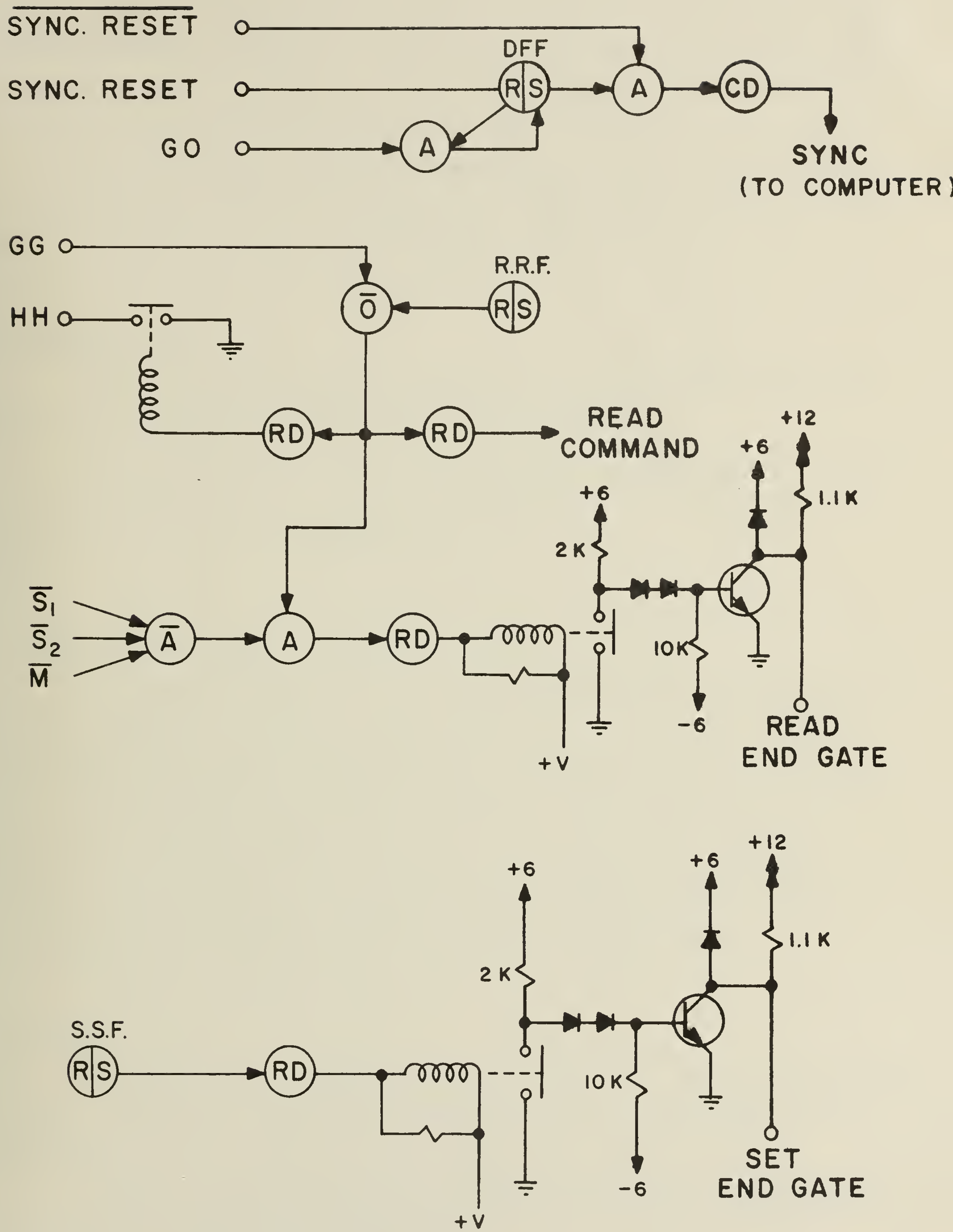
G2RG	M bit in the instruction
G2R'G	L bit in the instruction
G2R(B)G	$SFF \cap S_1FF$
G2R(C)G	$SFF \cap S_2FF$
G2CG	$RFF \cap$ channel $FF \cap BDI \cap GO$
G3CG	$RFF \cap \overline{\text{channel FF}} \cap BDI \cap GO$

2.9 End Signals

End signals, such as Local Set End, Read End, and the signal from the DFF (actually the sync signal) are shown in Fig. 17.

Local Set End signal comes from SFF through a slow-operating relay contact and returns to the reset side of the SFF and also to the set side of RFF.

The Read End signal comes from RFF through the AND gate with the "measure end" signal (the output of this AND gate is the read command signal and holds the display of the 6R1), and is fed back to the reset side of the RFF.



$\overline{\text{SYNC. RESET}}$
SYNC. RESET
GO
DFF
R S
A
A
CD
SYNC
(TO COMPUTER)
GG
HH
$\overline{O}$
R.R.F.
R S
RD
RD
READ
COMMAND
+12
+6
1.1 K
+6
2 K
$\overline{S_1}$
$\overline{S_2}$
$\overline{M}$
$\overline{A}$
A
RD
10K
-6
READ
END GATE
+V
+12
+6
+6
1.1 K
2 K
S.S.F.
R S
RD
10 K
-6
SET
END GATE
+V

FIGURE 17.

As was explained above, the Read End signal is inhibited by the signal $\bar{S}_1 \cap \bar{S}_2 \cap M$ until the START/STOP key resets RFF. These inhibition circuit and OR gates are included in the RFF. (The original flipflop circuit contains three "two-input AND" gates followed by a "three-input OR" gate. In this application two of them are connected to the reset side of the flipflop.)

DFF is set by the GO signal. The output of this flipflop is connected to the AND gate with $\overline{\text{SYNCR}}$. This output gives a SYNC signal to the computer and the DFF is reset in turn by the "SYNCR" signal (see Fig. 17).

2.10 Hang-Up Signal

Hang-up information is given in the classification bits of the first quarter word. When hang-up is indicated, processing stops.

The hang-up signal is sent from the computer when the Set cycle cannot be terminated because of the divergence or saturation of measured error. The hang-up FF is reset by the START/STOP key.

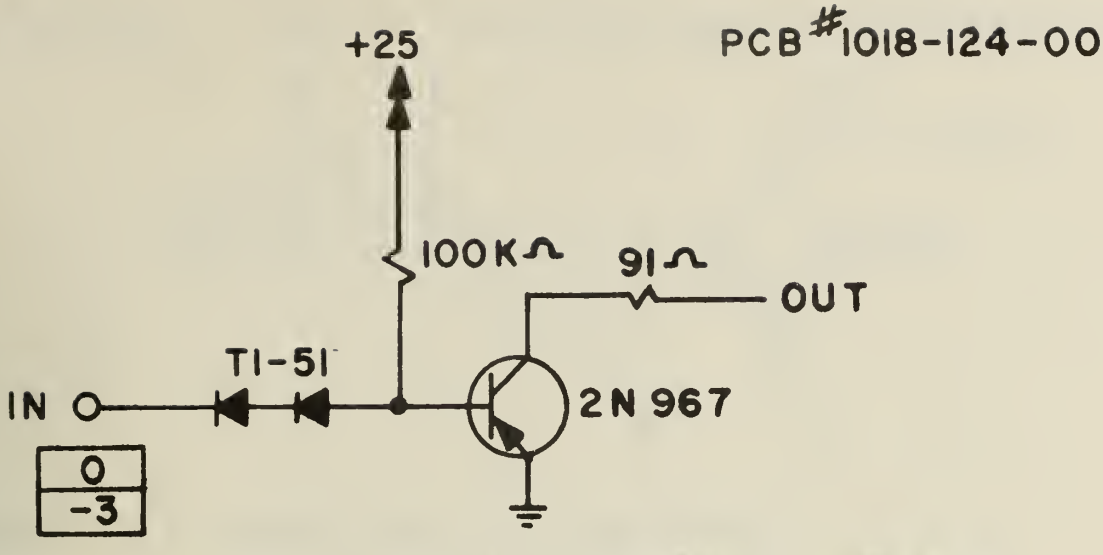
2.11 Digital Circuits and Semiconductor Devices

Logic elements selected are the npn planar epitaxial passivated silicon transistor, 2N706A; the diffused silicon mesa diode TI255 (for logic), and the TI51 and 1N750 diodes (for level shifting). In most of the logical design, gate drivers have been selected to be the NAND circuits. NOR circuits are used only in the decoder and matrix type circuitry. These circuits were originally designed for ILLIAC III, but for that purpose the transistor has now been replaced by the 2N2369 and the logic diode by the FD100. Figures 18 through 25 give all logic circuit topologies used in the Test Console.

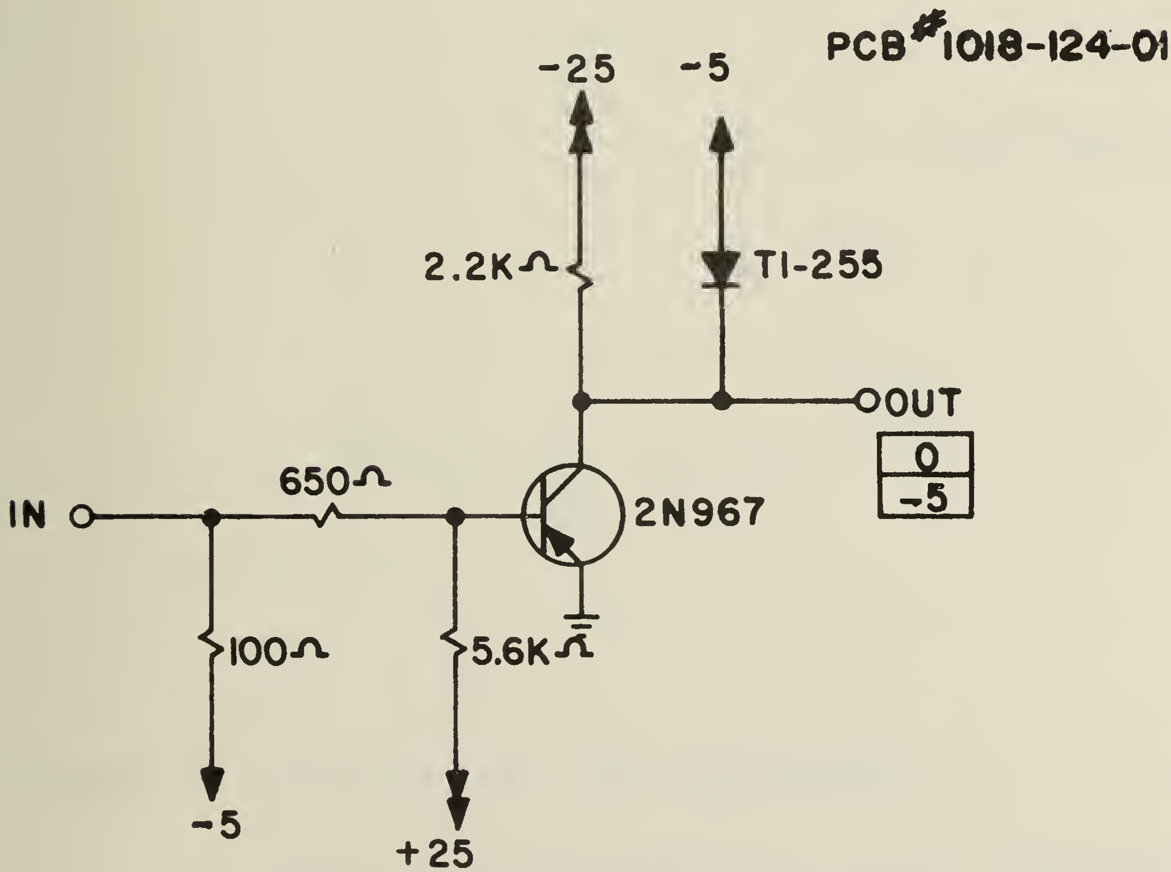
2.12 Relays

High sensitivity reed relays, having a 2-ma coil current and 9,500-ohm resistance, are used for information takeout from the type 6R1 digital scope plug-in unit.

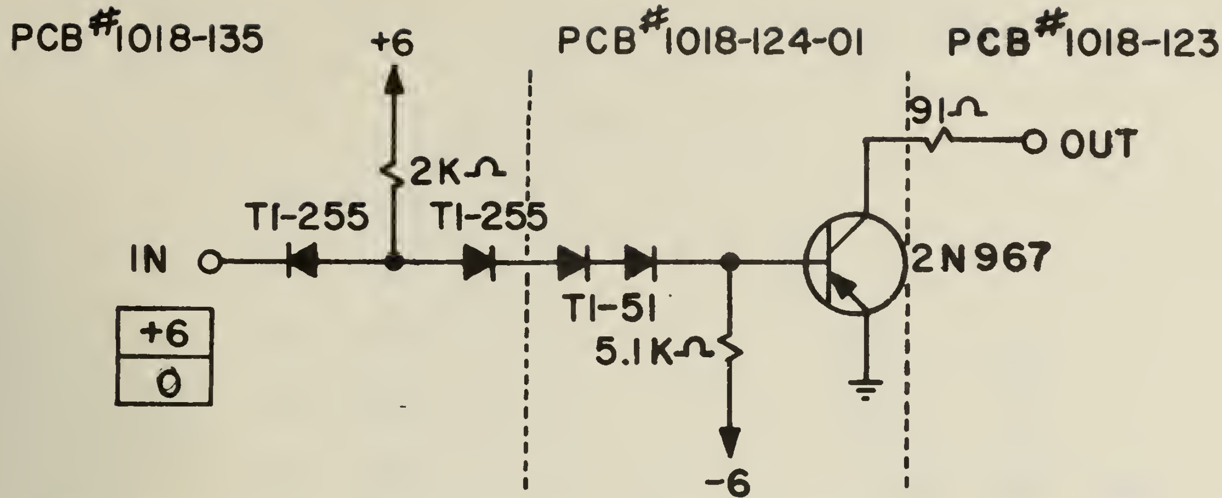
Relays for other purposes are also reed relays, the following models having been used: CR12Z, CR8Z, CR2Z, CRZ.



NOTE: ALL RESISTORS 5% TOLERANCE
CABLE DRIVER (AT ILLIAC II)
FIGURE 18



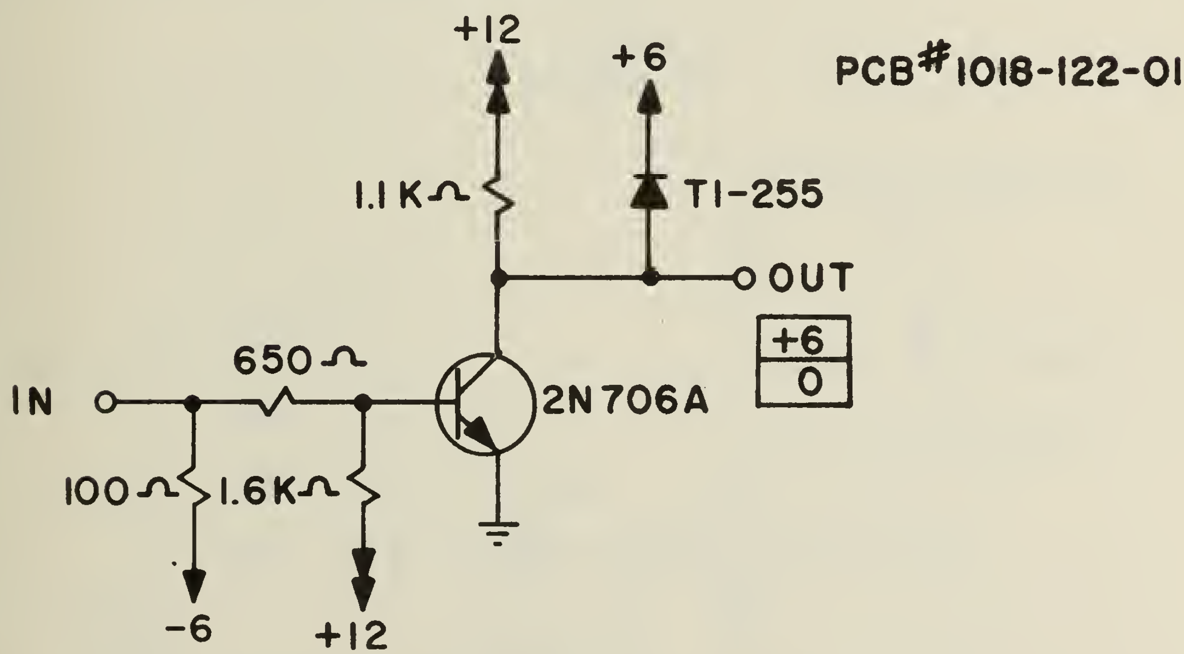
NOTE: ALL RESISTORS 5% TOLERANCE
CABLE TERMINATOR (AT ILLIAC II)
FIGURE 19



NOTE: ALL RESISTORS 5% TOLERANCE

CABLE DRIVER (AT TEST CONSOLE)

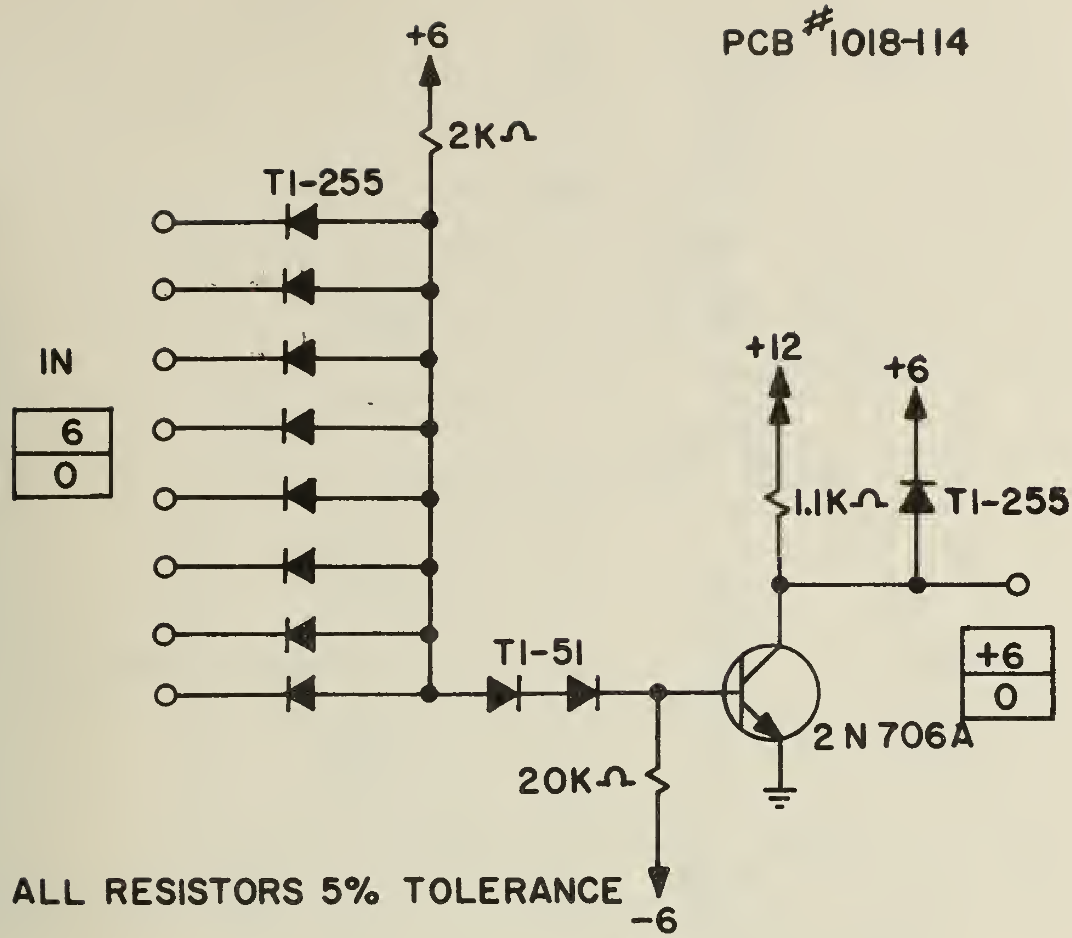
FIGURE 20



NOTE: ALL RESISTORS 5% TOLERANCE

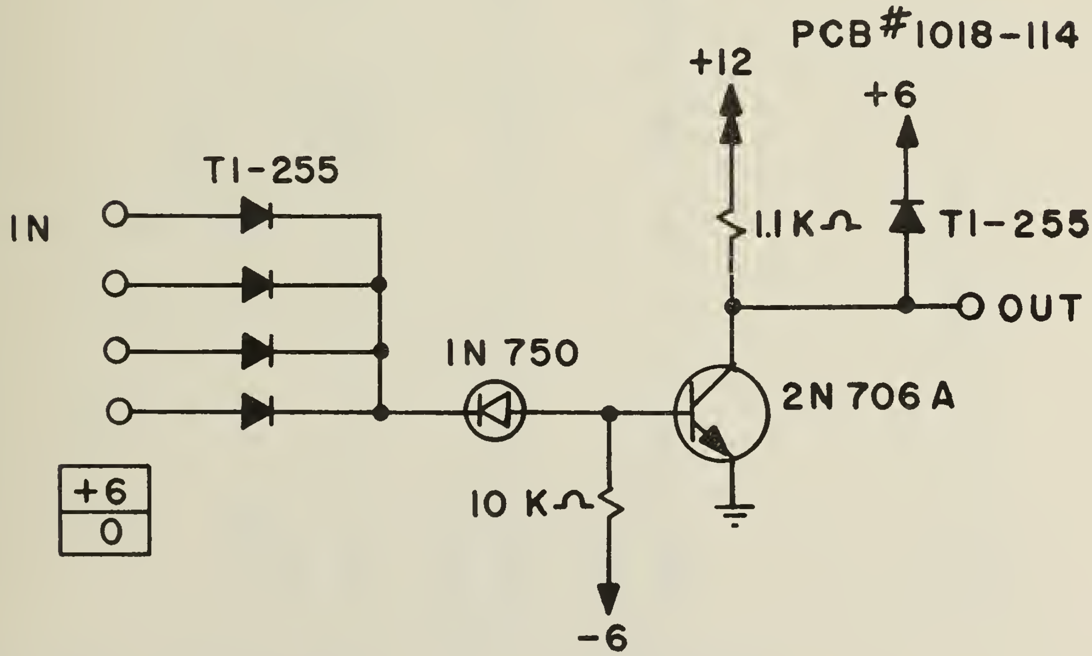
CABLE TERMINATOR (AT TEST CONSOLE)

FIGURE 21



NOTE: ALL RESISTORS 5% TOLERANCE

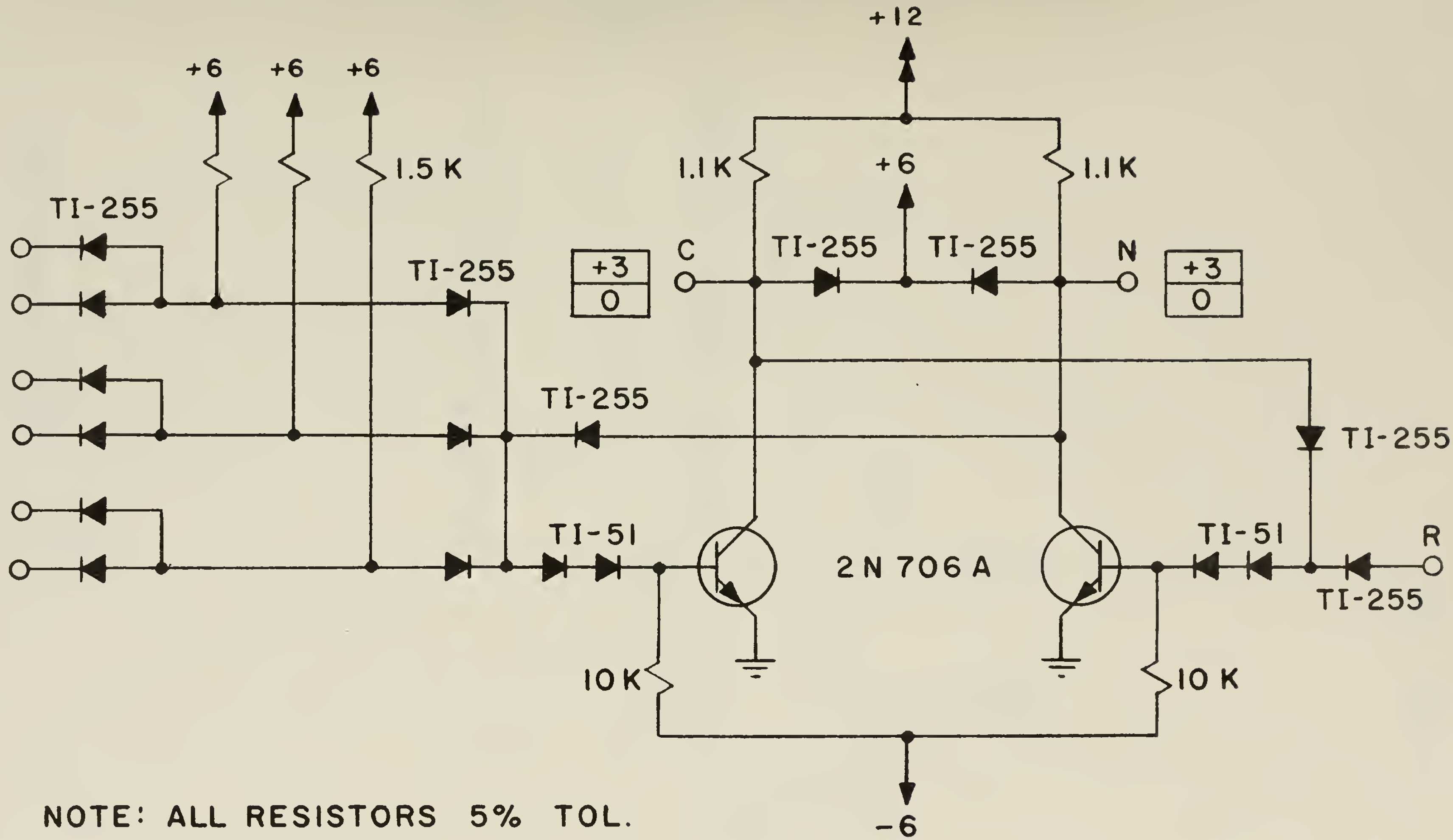
NAND
FIGURE 22



NOTE: ALL RESISTORS 5% TOLERANCE

NOR
FIGURE 23

PCB#: 1018-127

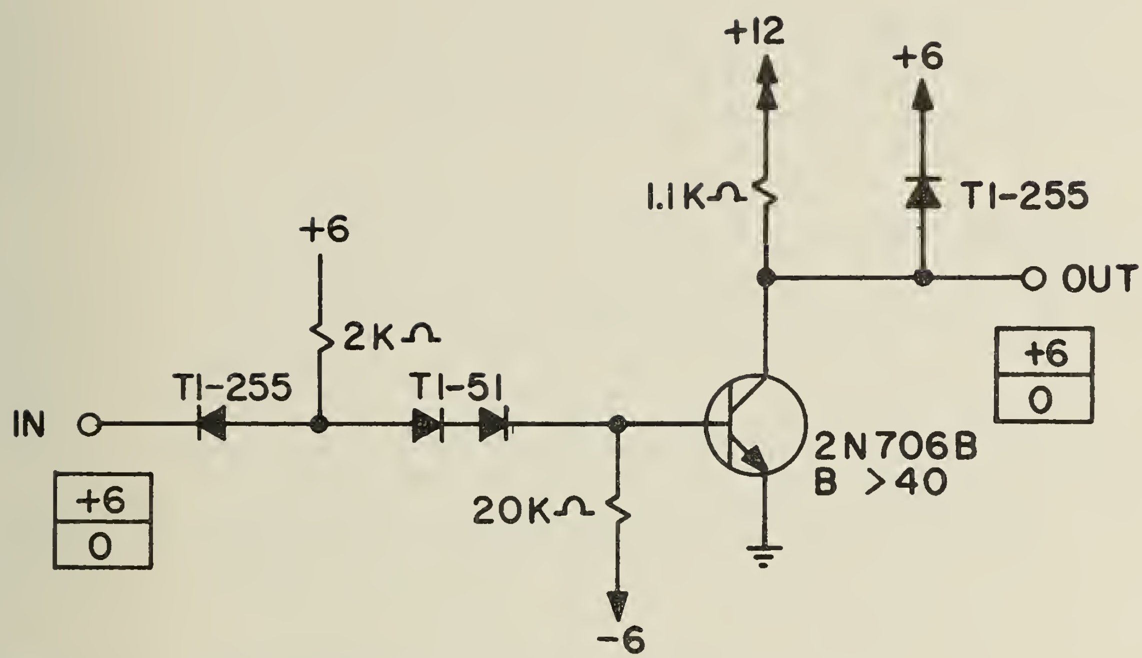


NOTE: ALL RESISTORS 5% TOL.

FLIPFLOP

FIGURE 24.

PCB 1018-114



NOTE: ALL RESISTORS 5% TOLERANCE

AND GATE DRIVER

FIGURE 25

2.13 Digital Readout Scope

The Tektronix Type 567 digital readout scope is the principal component of the digital readout in the machine. Measurement accuracy of the scope is ordinarily $\pm$ 3 per cent for both time and amplitude measurements. The least-significant digit can be ambiguous also. Minimum value of the input signal is 2 mv; minimum measureable time interval is 0.4 nsec.

2.14 Power Supply and Pulse Generator

A Tektronix Type 110 pulse generator is employed for time measurement. This pulse generator gives a 4 nsec rise and fall time, and a pulse width of up to 100 nsec with the voltage limited to one-half of the external power supply voltage.

The Tektronix Type 161 pulse generator, for dc measurements, gives 1 μsec rise and fall time and up to 1 msec pulse width. Output of this pulse generator is fed into a transistor stage. The output pulse voltage is equal to the supply voltage.

A Kepco power supply, suitably modified by a relay network (called Y_v), controls both the fast and slow pulse amplitude, as discussed previously. All resistances in the Y and Y_v networks have $\pm$ 2 per cent tolerance.